THE UNIVERSITY OF TEXAS AT AUSTIN   Date:__9/12/2016__

RECOMMENDATION FOR CHANGE IN ACADEMIC RANK/STATUS

Name:___Sun, Nan___ EID:__ns22375__ Present Rank:__Assistant Professor__

Years of Academic Service *(Include AY 2016-17 in each count)*:

At UT Austin since:_1/16/2011__(month/day/year) Total Years at UT Austin:__6.5__

In Present Rank since:_1/16/2011_(month/day/year) Total Years in Present Rank:__6.5__

Tenure-track only:
Number of Years in Probationary Status:__5__

Additional information:__Probationary Extension 2015-16__

Primary Department:_Electrical and Computer Engineering__

College/School: Engineering, Cockrell School of__

Joint Department:_N/A__

College/School: N/A__

Other Department(s):_N/A__

Recommendation actions[1]:

By Budget Council/Executive Committee:___Promote_____

Vote[2] for promotion_32; Against_0;·Abstain_2; Absent_0; Ineligible to vote_1

By Department Chair:___Promote_____

By College/School Advisory Committee:__Promote_____

Vote[2] for promotion_7; Against_0; Abstain_0; Absent_0; Ineligible to vote_0

By Dean: Promote_____

Administrative Action:___Promote to Associate Professor_____

Date Action Effective: September 1, 2017_____
(To be submitted to the Board of Regents as part of the annual budget.)

By:____[signature]____ Date:__December 15, 2016__
        For the President

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[1]See "Chart of Recommended Actions" for eligible recommended actions applicable to specific conditions and administrative levels.
[2]Record all votes for and against promotion, abstentions by eligible voting members, and the number of absent eligible voting members. The number of committee members ineligible to vote should also be recorded. Enter zero where it would otherwise be blank.

EVPP/4.15

EXHIBIT
P's 161

Dean's Assessment
Nan Sun
Department of Electrical and Computer Engineering
Cockrell School of Engineering

Dr. Nan Sun received his BS in Electronic Engineering from Tsinghua University in 2006. He received his PhD from Harvard University in Engineering Science in 2010. Dr. Sun joined the faculty in the Department of Electrical and Computer Engineering (ECE) at the University of Texas at Austin (UT) in January 2011. If successfully promoted to associate professor in September 2017, he will have accumulated five years of probationary service.

This is not an up-or-out case because the 2015-16 academic year did not count toward Dr. Sun's probationary service. The department decided to put the case forward one year prior to the mandatory review following a budget council vote in early spring.

Twelve external letters were submitted as part of the promotion dossier, of which, six writers were nominated by Dr. Sun, and six were selected by the budget council. Nine letter writers are faculty members at universities in the US: UC Berkeley, UCLA, UC San Diego, Colorado, Columbia, Michigan, Oregon State, Stanford, and Texas A&M. One is a member of the National Academy of Engineering (NAE). Two letter writers are faculty at international universities (IIT Madras and Toronto), and one is from industry (Texas Instruments).

Teaching

Dr. Sun's teaching has been in the area of integrated circuit (IC) design, which addresses the design, simulation, fabrication, and testing of circuits on a single chip. He has taught two undergraduate electives: EE 338K, *Electronic Circuits II* (taught once), and EE 338L, *Analog IC Design* (taught three times). EE 338L is cross-listed as a graduate course, EE 382M-14. Dr. Sun also taught an advanced graduate course on mixed-signal integrated circuit design, EE 382V, *Data Converters* (taught four times).

Dr. Sun's overall average undergraduate instructor rating of 4.63 is considerably higher than the corresponding values for assistant professors in ECE (4.21) and in the Cockrell School (4.17). At the graduate level, Dr. Sun's overall instructor rating is 4.84, which is considerably above the average for assistant professors in ECE (4.43) and in the Cockrell School (4.34). His CIS scores are indicative of his effective teaching style and concern for the students.

Senior faculty conducted peer evaluations of Dr. Sun's lectures five times, and each provided extremely positive assessments of his teaching style.

Research

Dr. Sun has made significant contributions in the field of analog and mixed-signal integrated circuit (IC) design. Specifically, he advanced the sub-areas of low-power analog techniques, time-domain signal processing, advanced analog-to-digital conversion techniques, frequency synthesis, and compressive sensing based analog front-ends. While his research addresses fundamental problems, Dr. Sun is interested in the translation of this work to several signal communication applications and consumer products.

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Highlights of Dr. Sun's research include:

- 23 archival journal papers (27 total) and 34 peer-reviewed conference proceedings (37 total) in rank. Fifteen of the journal papers were co-authored with his students.
- His publications have appeared in journals with impact factors (IF) that range from 9.4 (*Proceedings of National Academy of Science*) to 0.93 (*Electronics Letters*).
- Co-author of four book chapters.
- An h-index of 12 (Google Scholar) with 489 career citations.
- Three patent applications pending in rank

Dr. Sun's publication record increased significantly during the second part of his probationary period after the University of Texas signed an agreement with the leading IC foundry, Taiwan Semiconductor Manufacturing Company (TSMC). Dr. Sun needs a foundry to manufacture the integrated circuits that he designs.

While in rank, Dr. Sun has secured $3.4 million in external funding, of which approximately $1.7 million is his share. His funding includes three grants from the National Science Foundation (NSF), two of them as PI. One of grants is an NSF CAREER Award on "Combining Nuclear Magnetic Resonance with IC Technology." He also teamed with Dr. Nanshu Lu (Department of Aerospace Engineering and Engineering Mechanics) and a group of researchers at the University of Washington on an NIH grant related to monitoring muscle activity after a neurologic injury.

Dr. Sun has received research grants and gifts from industry, including Samsung, Texas Instruments, Cirrus Logic, and Intel. He has also received in-kind funding in the form of 11 free silicon fabrication shuttles, corresponding to a value of more than $0.7 million ($0.5 million his share).

The external references highlighted the innovative aspects of Dr. Sun's work and noted his creativity. Representative comments are summarized below:

Gabor C. Temes[1] (Oregon State, NAE) writes, "I found Dr. Sun's productivity highly impressive. The number of his publications in highly-regarded and selective journals and conferences is very high." And he concludes with this prediction: "Extrapolating from the 5-year record of Prof. Sun, I predict an exceptionally successful future career for him."

Shanthi Pavan[2] (Indian Institute of Technology Madras, Indian National Academy of Engineering) provides a revealing comment about Dr. Sun's early "work, nicknamed the 'pocket NMR', made waves in the IC design community for its ingenious application of IC technology to an area finding applications in diverse fields, ranging from chemical analysis to biosensing." He adds that "I distinctly remember, while reading Nan's papers on this subject 6 or 7 years ago, saying to myself this author is going to go far." Pavan compares Dr. Sun's research output with others in his worldwide cohort, "I have no hesitation in saying that Nan is among the best of the best. In fact, I cannot think of another assistant professor who has performed so well in a particularly difficult area like data-conversion." Pavan concludes: "In summary, Nan Sun is simply outstanding - I have been following his work for about 7 years now. In a less formal document, I would have said that his case for tenure is a no-brainer."

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[1] Professor, School of Electrical Engineering and Computer Science
[2] Professor, Department of Electrical Engineering

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David J. Allstot[3] (UC Berkeley) writes: "He impressed me with his world-class blend of creativity, analytical capabilities, experimental acumen, and breadth. His NMR work, for example, has combined deep aspects of physics, molecular engineering, signal processing, and analog/mixed-signal IC design." Concerning his research productivity and the quality of his work, Allstot notes: "The quantity of Prof. Sun's production is impressive. Many of us evaluate productivity informally based on an expectation of two archival journal papers and four conference papers per year measured over a number of years determined by the Ph.D. graduation year. Prof. Sun received his Ph.D. in 2010 so with 26 archival journal papers and 36 conference papers, he easily exceeds this difficult metric." Allstot concludes by offering the "strongest possible support for promotion to Associate Professor with indefinite tenure."

Boris Murmann[4] (Stanford) praises Dr. Sun's work on digitally assisted analog circuits by stating that it... "contains unique and new ideas that have brought these algorithms from an academic curiosity to a state that is now much more applicable to actual products." He goes on to state, "Dr. Sun's group has published a number of creative ideas."

The letters written by Ian Galton[5] (UC San Diego) and Edgar Sanchez-Sinencio[6] (Texas A&M) were generally positive and recommended promotion, but raised a few concerns.

- Galton questioned why Dr. Sun chose to publish several papers in rank in the lower impact factor journals IEEE *Transactions on Circuits and Systems II: Express Briefs* (IF=1.1) and IEEE *Electronics Letters* (IF=0.93), rather than in the IEEE *Journal of Solid-State Circuits* (JSSC) (IF=3.3) or the IEEE *Transactions on Circuits and Systems I: Regular Papers* (IF=2.4).
- Sanchez-Sinencio recommended that Dr. Sun "increase the number of publications in top journals."
- Galton also advised "Professor Sun to write such papers (in high-impact journals) in a more balanced, analytical fashion. Many of his papers contain good ideas, but they sometimes contain sweeping statements, often without proof, about the benefits of his ideas and the drawbacks of previously published techniques."

Advising and Student Mentoring
Dr. Sun has graduated four PhD (one co-supervised) and 14 MS students, and one former student is currently an assistant professor at the University of Buffalo. Dr. Sun is currently supervising 11 PhD students (two co-supervised) and two MS students.

University Service
Dr. Sun has served on the Parking and Traffic Appeals Committee at the university level and on five departmental committees, including the future of ECE curriculum reform committee, the ECE integrated circuits and systems area graduate admissions committee, and two faculty search committees. In addition, he has been the organizer for the ECE integrated circuits and systems seminar series since 2011.

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[3] Professor in Residence, Department of Electrical Engineering and Computer Science (formerly Department Chair, Department of Electrical Engineering, University of Washington)
[4] Professor, Department of Electrical Engineering
[5] Professor, Department of Electrical and Computer Engineering
[6] Endowed Chair, Department of Electrical and Computer Engineering

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Professional Service

Dr. Sun has been active in several professional organizations and has served on various organizing committees. He is an associate editor for the *IEEE Transactions on Circuits and Systems I: Regular Papers* and a member of the editorial board for the *Journal of Semiconductors*. He has served as a member of the technical program committee for the Custom Integrated Circuits Conference, continuously since 2012 and for the Asian Solid-State Circuits Conference during the same period. Dr. Sun serves as the vice chair of the Central Texas Joint Chapter of the IEEE Solid-State-Circuits Society and the Circuits-and-Systems Society.
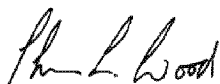
Other Evidence of Merit or Recognition

Dr. Sun received a CAREER Award from the National Science Foundation in 2013. In addition, his work has been featured in the scientific and popular press, including the *EE Times, R&D Magazine, Electronics Weekly*, and the *MIT Technology Review*.

Overall Assessment

Dr. Sun has established a strong research program in a mature field, and he is moving into the highly promising field of analog sensor design. His work has shown wide applicability in various application spaces, and he has developed deep relationships with industry, as evidenced by the recurring financial support provided by several companies for his research endeavors. Reference letters are overwhelmingly positive. While a few reviewers made suggestions to improve the impact of his publications, all recommended promotion. Dr. Sun has proven to be an excellent teacher and mentor. His record of service is solid.

The Cockrell School Promotion and Tenure Committee discussed the concerns expressed in the letters at length. In the end, they agreed with the department chair's and budget council's assessments and unanimously supported promotion.

Overall, I believe that Dr. Sun's performance meets or exceeds expectations for promotion to associate professor with tenure in all categories, and I support this case without reservation.

Sharon L. Wood, Dean
18 October 2016
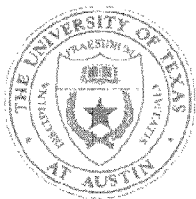
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ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
Cockrell School of Engineering

1616 Guadalupe St. • UTA Building, 7th Floor • Austin, Texas 78701
http://www.ece.utexas.edu/

September 30, 2016

Chair's statement regarding updated Curriculum Vitae submitted by Prof. Nan Sun on September 29, 2016

Prof. Sun submitted an updated curriculum vitae on September 29 to i) correct an error in the CV that had originally been submitted with the promotion dossier and ii) update the status of one of his papers.

- The original CV submitted by Professor Sun listed him as an associate editor for the *Journal of Semiconductors*. He actually is on the editorial board of the Journal and is not an associate editor. This, in my judgment, was an honest mistake due to an incorrect translation from Chinese to English.
  This service position did not receive much attention in our deliberations because the Journal appears to have a mostly geographically limited readership and editorial board, moderate impact and is not in our judgment a first-tier publication.
- Since the original submission of the promotion package, Prof. Sun's paper "A 12b ENOB, 2.5MHz, 4.8mW VCO Based 0-1 MASH with Direct Digital Background Calibration" was accepted for publication in the Journal of Solid State Circuits. The acceptance email is attached. My own chairman's letter refers to this paper as being accepted.

Sincerely,

Prof. Ahmed H. Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
Cockrell School of Engineering
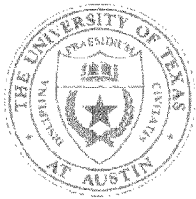
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November 4, 2016

Chair's letter in support of the promotion of Prof. Nan Sun to the rank of associate professor with tenure

Prof. Sun joined the Department of Electrical and Computer Engineering in January 2011. If promoted to associate professor in September of 2017, he will have served as an assistant professor at the University of Texas at Austin for six and a half years. However, this is technically an early promotion case because Prof. Sun had requested an extension to his probationary period due to childbirth.

Nan is a recognized innovative researcher in analog circuit design, a field where it is increasingly difficult to come up with creative ideas with potentially high impact because of the maturity of the field and the sheer amount of industrial research and development efforts focused on this field. Nan is also resuming his no less creative research in the emerging area of analog sensing. The Budget Council recognized his strong accomplishments and potential, and determined that he meets all expectations for promotion at the premier departments of Electrical and Computer Engineering in the nation by a vote of 32 YES, 0 NO and 2 ABSTAIN and 1 INELIGIBLE TO VOTE. The abstain is the departmental representative serving on the Cockrell School of Engineering promotion and tenure committee. He abstained and explained that he did not want to vote twice on the same case. The ineligible is myself. Our associate professors voted 17 YES, 1 NO and 0 ABSTAIN in support of promotion. The negative vote reflected concerns similar to the criticism leveled explicitly or implicitly in some of the reference letters and discussed below.

Third Year Review

The third year review conducted by peers noted that Prof. Sun was making satisfactory progress in his research and teaching. In particular, it praised him for receiving a National Science Foundation CAREER award, additional substantial funding from the National Science Foundation and industry, publishing nine journal and 11 conference papers and giving numerous invited lectures. In addition, it noted that he is an outstanding teacher, as evidenced by his teaching scores, students' comments and peer teaching evaluations.

Teaching Load

The normal teaching load for a tenure-track assistant professor is two courses per academic year plus supervision of a senior design team for two semesters. One of the courses must be an undergraduate course. This requirement is waived only under exceptional circumstances if the department has unmet needs at the graduate level. Faculty in the department are routinely given modified instructional duties upon the birth of a child.

Special note about reference letter from Prof. Sanchez

As noted in a Budget Council statement (located in the Supplemental Materials folder), the reference letter by Prof. Sanchez makes several factual errors despite the fact that Prof. Sanchez had access to Prof. Sun's CV and statements. My colleagues and I have dismissed this letter in our deliberations.

Teaching

By any measure, Prof. Sun is an excellent teacher. Since he arrived at UT, he has taught our core undergraduate and graduate courses in analog and mixed signal design. Nan completely redesigned EE438K, our core undergraduate course in this area, changing the lectures to reflect the current state-of-the-art, developing more challenging homework and most importantly, introducing an open ended design project. Similarly, he created new homework assignments in 382M/338L-14, our fundamental undergraduate and graduate analog integrated circuit (IC) design courses, which are cross listed because of lack of technical expertise in this area at UT, and also introduced an open ended design project. Finally, he redesigned EE 382M-24 Data Converters and introduced a student design contest. It's important to note that Prof. Sun has also raised industrial funding to support these courses, and several of his student teams have placed well in international analog circuit design competitions sponsored by Texas Instruments.

Prof. Sun's accomplishments in revamping our analog circuit design courses were very well received by our students, as evidenced by his high instructor scores which range from 4.3 to 5. Students praise his teaching and the fact that he cares about his students. Indeed, the following quotes summarize many of the comments he has received: "Your teaching style is very organized and you explain the material clearly. Also, you seem to care about the progress of students" and "extremely enthusiastic, very dedicated and <u>receptive</u> to students." The peer evaluations also paint the picture of a highly energetic, engaged and enthusiastic teacher who is very well organized and has a deep knowledge of the material.

Research

Nan has achieved recognition as an innovative researcher in mixed signal design. This is no mean feat, as observed by several reference letter writers and noted by Prof. Galton (UC San Diego) who states that "These aspects of the field make it very difficult to innovate meaningfully, so it is laudable that Professor Sun has managed to make multiple contributions to date."

While at UT, Prof. Sun has made several notable contributions to high-performance and ultra-low-power analog IC design that have the potential of changing the way analog circuits are designed. All of these contributions are in areas unrelated to his PhD work or the work of his PhD advisor. Three of these contributions in particular were highlighted in almost all the reference letters we received.

As noted by Prof. Murmann (Stanford), his work on digitally assisted analog circuits "contains unique and new ideas that have brought these algorithms from an academic curiosity to a state that is now much more applicable to actual products." This work is particularly important because of the non-idealities in nanoscale analog circuits that result from current imperfect fabrication techniques at these challenging scales and the fact that the detrimental effect of these non-idealities is amplified by the use of lower voltages to achieve lower power consumption. While Nan did not introduce the concept of using digital signal processing to overcome non-idealities in analog circuits, his work substantially improves on the state-of-the-art in terms of reduced power and hardware requirements, and exhibits faster convergence speed. It is no

surprise that industry aggressively pursued his PhD student who worked on this problem and hired him before he even completed his thesis.

His work on mismatch shaping techniques also addresses the shortcomings of fabrication technology at the nanoscale. The mismatch problem is particularly critical in highly linear analog to digital and digital to analog converters. Nan developed and analyzed clever extensions of current dynamic element matching techniques that, unlike the state-of-the-art, effectively solve static mismatch between circuits elements and mitigate dynamic transition errors. His work was based on the insightful realization that by maintaining a constant transition rate, one can turn dynamic errors into a signal independent offset that can then be corrected. Commenting on this work, Prof. Galton notes that the work exhibits "creativity and appear to offer significant advantages."

Finally, I note his work on ultra-low power high-performance successive approximation analog to digital converters. In addition to proposing similar clever designs for this class of analog-to-digital converters, Nan was the first researcher to use statistical estimation theory in the design of such converters. Prof. Flynn (Michigan) notes that this "research on ADCs has led to solid results." Prof. Murmann praises this work stating that "Dr. Sun's group has published a number of creative ideas."

Nan's innovative contributions are recognized by his peers, as clearly demonstrated by the remarkably high number of invited talks for a researcher of his age that he has given at well-known corporations and academic institutions.

Prof. Sun is very well funded by highly competitive peer-reviewed grants from NSF and NIH. He has received an NSF Career Award and several industry gifts or awards. I expect his funding to increase even further as a result of his new research directions.

While all the reference letter writers praised his innovative work and recommended that he be promoted to the rank of associate professor with tenure, a few letters either explicitly or implicitly raised three issues: i) quality of his writing, ii) relatively small number of publications in the IEEE Journal of Solid-State Circuits (JSSC) and iii) the future of his research in a rapidly maturing field. I have discussed these issues with my colleagues and Nan as we debated whether to consider his promotion case this year or postpone it to next. I agree with my colleagues that Nan should be promoted this year and that these issues are not significant. The first issue was raised by only one reference letter writer, Prof. Galton. I have had the opportunity to discuss this issue further with Prof. Galton over the phone. Prof. Galton has very high regard for Nan and wants to make sure that his writing measures up his creativity and clever designs. According to Prof. Galton, Nan's PhD advisor may not have provided him with effective mentoring. To address this issue, Prof. Gharpurey, who is known for his very careful writing and is a highly regarded researcher in RF analog circuit design, has agreed to work with Nan on his future writings. Nan has welcomed this active support from the department. I also note that the papers that Prof. Galton refers to were all peer-reviewed. The mere fact that they were published in well-recognized journals and conferences indicated to my colleagues and me that the reviewers and editors did not agree with Prof. Galton's view that Nan sometimes makes "sweeping statements." The second issue is also not a concern because as Prof. Kinget (Columbia) noted "work includes prototyping these techniques in integrated circuits. This is an essential step, but also a costly and time-consuming step. Going from theoretical idea, through circuit realization, simulation, layout and tape-out, and finally to experimental evaluation in the lab can easily take 1.5 years for one trial." It's worth noting in this context that Nan did not get access to the TSMC fabrication shuttles until well into his third year at UT. The agreement between UT and TSMC was held up by UT for two years and was brought to my attention in December 2012. Working

with our then VP of research, Prof. Juan Sanchez, and Bill Cattlet we finally managed to get the agreement signed in June 2013. This lack of access to fabrication made it impossible for him to publish in certain conferences and journals such as JSSC. However, I note that he has published two papers in JSSC while at UT, one of which was accepted for publication this month after our BC vote. He also has one more paper in the final round of reviews in JSSC. That paper has been accepted for publication with minor revisions also this month. In addition, Nan has extended several of his recent well-received fabricated chips conference papers into journal papers. He has submitted one paper this month to JSSC and is close to finishing the second one, which we expect him to submit to the same journal by the end of October. Finally, I note that the reviewers did not have access to the final version of Nan's research statement. As such, they were unable to evaluate his future directions. Nan is clearly resuming his groundbreaking work on medical analog sensors, work that started with his PhD. He has already secured funding on this topic from NSF and NIH. In addition, he is a regular participant in our monthly roundtable discussions with our colleagues in the medical school. These roundtable discussions focus on developing novel techniques for healthcare delivery that are based on nonintrusive sensing of a subject's physiological conditions. I expect him to play a leading role in all of the research initiatives that will come out of these discussions.

Our department has adopted the practice of comparing each colleague with his or her most prominent peers at the first-tier departments in Electrical and Computer Engineering, such as MIT, Stanford, the University of California Berkeley, the University of Illinois Urbana-Champaign (UIUC), Georgia Tech, Caltech and Princeton. I selected Associate Profs. Sudhakar Pamarti (UCLA), Jeyanandh Paramesh (CMU) and Ada Poon (Stanford) to be the peer comparison group for Nan. Pamarti, Paramesh and Poon were promoted to the rank of associate professor in 2010, 2012 and 2013 respectively. Nan compares favorably to all three associate professors. In particular, the comparison shows that Nan has published more journal papers and conference papers than all three associate professors at the time of their promotion. His career h-index is close to those of Pamarti and Poon despite the fact that they are more senior, having received their PhDs in 2003 and 2004 respectively, and equal to that of Paramesh, who received his PhD in 2006. Indeed, his h-index based on papers published in or after 2011 is equal to that of Murmann also for papers published in the same time period and higher than that of Pamarti for the same period. It's important to note that Murmann writes regular highly-regarded reviews of the state-of-the-art in analog circuit design that garner many citations. I also note that Profs. Pamarti and Murmann themselves provided their own comparisons with peers in the field who they considered to be the best at Nan's career level and who are currently faculty members at the University of Southern California, University of Toronto and University of Florida, and concluded that Nan is as good or better than everyone they mentioned.

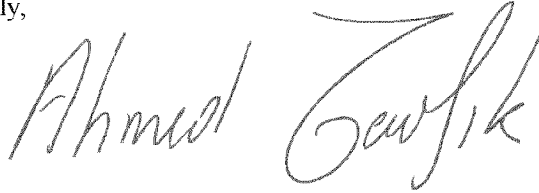## Service

Nan has provided excellent service to both UT and the profession. Details can be found in his resume and the budget council statement. I will note in particular that Nan played a key role several times on our faculty recruiting committees. These committees are labor intensive as they require proactive outreach and recruiting efforts across the multiple areas spanned by the department.

Summary

Nan is an excellent teacher and a highly creative researcher in analog circuit design who is moving beyond the traditional and mature problems in the field to the highly promising field of analog sensor design. He has served UT and his profession well. Echoing what other letter writers said in supporting Nan's promotion, Prof. Kinget states that Nan is "launching a number of important new research activities. In combination with his research and teaching accomplishments achieved in the past five years, I am confident that he will continue to grow his profile and establish his prominence in the solid-state circuit design research community." I strongly endorse his promotion to associate professor with tenure.

Sincerely,

Prof. Ahmed H. Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering

Research

Professor Nan Sun has been in UT Austin since 01/2011. Within the past 3 year Professor Sun has published 9 peer-reviewed journal articles and 11 conference papers. Dr. Sun also delivered 25 invited talks in various places.

He has won the NSF CAREER Award in 2013. He has obtained $700K funding, from NSF and industry (TI, Samsung, Intel, etc.). He is supervising a large number students, including 6 full-time and 7 part-time PhD students and 6 MS Thesis/Report students. Since he is at UT for only three years, this shows very good trajectory and student pipeline.

Teaching:

Professor Sun has been teaching in our department for 3 years. Within the review period, professor Sun has taught EE338K, EE338L (undergraduate courses) and EE 382V – Data Converters (graduate course). The teaching evaluation for the past 3 years are summarized in the following:

Year	2011	2011	2012	2012	2013	2013
Semester	Spring	Fall	Spring	Fall	Spring	Fall
Course	4.5	NA	4.9	4.3	4.8	
Instructor	4.8	NA	5.0	4.5	4.9	

Average CIS Score for U/G =4.01, for Grad = 4.19
Department Average CIS Score for U/G = 4.07, for Grad = 4.22

Prof. Sun's teaching evaluation is outstanding. He also raised continuous funding support from Texas Instruments to turn his class projects into student designer contests with total prize money of $10K over the past three years.

The peer teaching evaluation was done by Prof. Hao Ling on April 4, 2012, concluding that Prof. Sun is a very engaging and enthusiastic teacher.

Service:
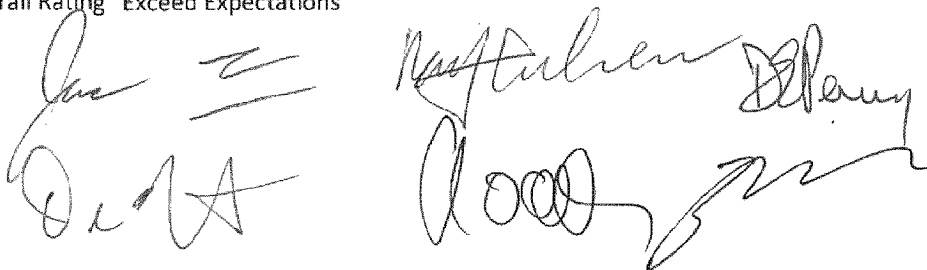
Professor Sun has served as Vice Chair of IEEE Central Texas SSC/CAS Chapter, TPC member for ASSCC, NSF panelist, and frequent reviewer for many journal and conferences. He also served in UT and the ECE department in the following roles.

- ECE Graduate Admission Committee in ICS Area
- Graduate Site Visit coordinator for ICS Area
- Member in UT Austin Parking and Traffic Appeals Committee

Summary

As a new faculty member, Dr. Nan Sun has jump-started his research group at UT, and made excellent contributions to both the teaching and research programs in the ECE Department. The quality of his work is outstanding and the department is fortunate to count him as a member of the faculty.

Overall Rating "Exceed Expectations"

Electrical and Computer Engineering   Revised September 29, 2016

THE UNIVERSITY OF TEXAS AT AUSTIN
Cockrell School of Engineering
Standard Resume

FULL NAME: Nan Sun   **TITLE:** Assistant Professor

DEPARTMENT: Electrical and Computer Engineering

EDUCATION:

Harvard University	Engineering Science	Ph.D.	2010
Tsinghua University	Electronic Engineering	B.S.	2006

CURRENT AND PREVIOUS ACADEMIC POSITIONS:

University of Texas at Austin	Fellow, AMD Endowed Chair in Computer Engineering	Aug. 2013 – present
University of Texas at Austin	Assistant Professor	Jan. 2011 – present

OTHER PROFESSIONAL EXPERIENCE:

Texas Instruments	Visiting Professor	Jul. 2013 – Aug. 2013

CONSULTING:

Cirrus Logic	Consultant	May 2015 – present
Analog Devices	Consultant	Jul. 2014 – Oct. 2014

HONORS AND AWARDS:

- IEEE Senior Member, 2016
- Jack Kilby / Texas Instruments Endowed Faculty Fellowship in Computer Engineering, 2015-2016
- IEEE Circuits-and-Systems Society Chapter of the Year Award, 2014
- Fellow of the AMD Chair in Computer Engineering, 2013-present
- NSF CAREER Award, 2013

MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES:

- Senior Member, Institute of Electrical and Electronics Engineers (IEEE), 2011-present

UNIVERSITY COMMITTEE ASSIGNMENTS:

Departmental-	ECE curriculum reform committee	2016-present
	ECE colloquium committee	2015-present
	ECE junior faculty search committee	2015-present
	ECE integrated circuits and systems (ICS) area graduate admission committee	2011-present
	ECE ICS area seminar organizer	2011-present
	ECE Silicon Laboratories Endowed Chair search committee	2014-2015

1

Electrical and Computer Engineering   Revised September 29, 2016

University-   University parking and traffic appeals committee   2012-2014

PROFESSIONAL SOCIETY AND MAJOR GOVERNMENTAL COMMITTEES:

2016-present: Associate Editor for *IEEE Trans. on Circuits and Systems – I, Regular Papers*
2016-present: Editorial Board Member for *Journal of Semiconductor*
2016-present: Technical program committee member in *Custom Integrated Circuits Conference*
2012-present: Technical program committee member in *Asian Solid-State Circuits Conference*
2012-present: Vice Chair of IEEE Central Texas Solid-State-Circuits Society Chapter
2012-present: Vice Chair of IEEE Central Texas Circuits-and-Systems Society Chapter
2012-present: Proposal review panelist for National Science Foundation (NSF) for 4 times

PUBLICATIONS: *underlined names indicate students I advised or co-advised at UT

A.   Refereed Archival Journal Publications

1.   David Ricketts, Xiaofeng Li, **Nan Sun**, Kyoungho Woo and Donhee Ham, "On the self-generation of electrical soliton pulses," *IEEE Journal of Solid-State Circuits,* vol. 42, no. 8, pp. 1657-1668, August 2007.
2.   **Nan Sun**, William Andress, Kyoungho Woo, and Donhee Ham, "Surpassing tradeoffs by separation: examples in transmission line resonators, phase-locked loops, and analog-to-digital converters," (invited paper) *Journal of Semiconductor Technology and Science*, vol. 8, pp. 210-220, Sept. 2008.
3.   **Nan Sun**, Hae-Seung Lee, and Donhee Ham, "Digital background calibration in pipelined ADCs using commutated feedback capacitor switching," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 55, no. 9, pp. 877-881, Sept. 2008.
4.   **Nan Sun**, Yong Liu, Hakho Lee, Ralph Weissleder, and Donhee Ham, "CMOS RF biosensor utilizing nuclear magnetic resonance," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1629-1643, May 2009.
5.   **Nan Sun**, Tae-Jong Yoon, Hakho Lee, William Andress, Ralph Weissleder, and Donhee Ham, "Palm NMR and one-chip NMR," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 342-352, Jan. 2011.
6.   **Nan Sun**, "High-order mismatch-shaping in multibit DACs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 58, no. 6, pp 346-350, Jun. 2011.
7.   **Nan Sun** and Peiyan Cao, "Low-complexity high-order vector-based mismatch shaping in multi-bit $\Delta\Sigma$ ADCs," *IEEE Transactions on Circuits and Systems - II: Express Briefs*, vol. 58, no. 12, pp. 872-876, Dec. 2011.
8.   **Nan Sun**, "High-order mismatch-shaped segmented multibit delta-sigma DACs with arbitrary unit weights," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 2, pp. 295-304, Feb. 2012.
9.   Youngchun Kim, Wenjuan Guo, Vikrham Gowreesunker, **Nan Sun**, and Ahmed Tewfik, "Multi-channel sparse data conversion with a single analog-to-digital converter," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 2, pp. 470-481, Sept. 2012.
10. **Nan Sun**, "Exploiting process variation and noise in comparators to calibrate interstage gain nonlinearity in pipelined ADCs," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 4, pp. 685-695, Apr. 2012.
11. Arindam Sanyal and **Nan Sun**, "SAR ADC architecture with 98% reduction in switching energy over conventional scheme," *Electronics Letters,* vol. 49, pp. 248-250, Feb. 2013.
12. **Nan Sun**, Yong Liu, Ling Qin, Hakho Lee, Ralph Weissleder, and Donhee Ham, "Small NMR biomolecular sensors," *Journal of Solid-State Electronics* (invited paper), vol. 84, pp. 13-21, Mar. 2013.
13. Kareem Ragab, Mucahit Kozak, and **Nan Sun**, "Thermal noise analysis of a programmable-gain switched-capacitor amplifier with input offset cancellation," *IEEE Transactions on Circuits and Systems – II, Express Briefs,* vol. 60, no. 3, pp. 147-151, Mar. 2013.
14. Arindam Sanyal and **Nan Sun**, "An energy-efficient, low frequency-dependence switching technique for SAR ADCs," *IEEE Transactions on Circuits and Systems – II: Express Briefs,* vol. 61, no. 5, pp. 294-298, May 2014.
15. Arindam Sanyal, Peijun Wang, and **Nan Sun**, "A thermometer-like mismatch shaping technique with minimum element transition activity for multibit delta-sigma DACs," *IEEE Transactions on Circuits and Systems – II: Express Briefs,* vol. 61, no. 7, pp. 461-465, Jul. 2014.

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16. Dongwan Ha, Jeffrey Paulsen, **Nan Sun**, Yi-Qiao Song, and Donhee Ham, "Scalable NMR spectroscopy with semiconductor chips," *Proceedings of National Academy of Engineering (PNAS)*, vol. 111, no. 33, pp. 11955–11960, Aug. 2014.

17. Kareem Ragab, Long Chen, Arindam Sanyal, and **Nan Sun**, "Digital background calibration for pipelined ADCs based on comparator decision time quantization," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 62, no. 5, pp. 456-460, May 2015.

18. Manzur Rahman, Arindam Sanyal, and **Nan Sun**, "A novel hybrid radix-3/radix-2 SAR ADC with fast convergence and low hardware complexity," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 62, no. 5, pp. 426-430, May 2015.

19. Arindam Sanyal, Long Chen, and **Nan Sun**, "Dynamic element matching with signal-independent element transition rates for multibit delta sigma modulators," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 62, no. 5, pp. 1325-1334, May 2015.

20. Wenjuan Guo, Tsedeniya Abraham, Steven Chiang, Chintan Trehan, Masahiro Yoshioka, and **Nan Sun**, "An area and power-efficient Iref compensation technique for voltage-mode R-2R DACs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 62, no. 7, pp. 656-660, July 2015.

21. Dongwan Ha, **Nan Sun**, and Donhee Ham, "Next generation multidimensional NMR spectrometer based on semiconductor technology," *eMagRes*, vol. 4, pp. 117-125, 2015.

22. Arindam Sanyal and **Nan Sun**, "Dynamic element matching techniques for static and dynamic errors in continuous-time multi-bit delta-sigma modulators," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 598-611, Dec. 2015.

23. Kyoungtae Lee, Yeonam Yoon, and **Nan Sun**, "A scaling-friendly low-power small-area delta-sigma ADC with VCO-based integrator and intrinsic mismatch shaping capability," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 561-573, Dec. 2015.

24. Arindam Sanyal, Xueyi Yu, Yanlong Zhang, and **Nan Sun**, "Fractional-N PLL with multi-element fractional divider for noise reduction," *Electronic Letters*, vol. 52, no. 10, pp. 809-810, May 2016.

25. Long Chen, Kareem Ragab, Xiyuan Tang, Jeonggoo Song, Arindam Sanyal, and **Nan Sun**, "A 0.95-mW 6-b 700-Ms/s single-channel loop-unrolled SAR ADC in 40-nm CMOS," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, accepted.

26. Arindam Sanyal and **Nan Sun**, "A second-order VCO-based delta sigma ADC using a modified DPLL," *Electronics Letters*, vol. 52, no. 14, pp. 1204-1205, accepted.

27. Kareem Ragab and **Nan Sun**, "A 12b ENOB, 2.5MHz, 4.8mW VCO-based 0-1 MASH with direct digital background calibration," *IEEE Journal of Solid-State Circuits*, accepted.

B. Refereed Conference Proceedings

1. Yong Liu, **Nan Sun**, Hakho Lee, Ralph Weissleder, and Donhee Ham, "CMOS mini nuclear magnetic resonance system and its application for biomolecular sensing, " *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 140-141, Feb. 2008.

2. **Nan Sun**, Tae-Jong Yoon, Hakho Lee, William Andress, Vasiliki Demas, Pablo Prado, Ralph Weissleder, and Donhee Ham, "Palm NMR and one-chip NMR," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 6-8, Feb. 2010.

3. **Nan Sun**, Yong Liu, Hakho Lee, Ralph Weissleder, and Donhee Ham, "Silicon RF NMR biomolecular sensor – Review, " (invited paper) *IEEE Proceedings of International Symposium on VLSI Design, Automation & Test (VLSI-DAT)*, pp. 121-124, Apr. 2010.

4. Arindam Sanyal and **Nan Sun**, "A simple and efficient dithering method for vector quantizer based mismatch-shaped ΔΣ DACs," *IEEE Proceedings of International Symposium on Circuits and Systems*, pp. 528 - 531, May 2012.

5. **Nan Sun**, Hae-Seung Lee, and Donhee Ham, "A 2.9-mW 11-b 20-MS/s pipelined ADC with dual-mode-based digital background calibration," *Proceedings of European Solid-State Circuit Conference (ESSCIRC)*, pp. 269-272, Sept. 2012.

6. **Nan Sun**, Yong Liu, Ling Qin, Guangyu Xu, and Donhee Ham, "Solid-state and biological systems interface," *Proceedings of European Solid-State Circuit Conference (ESSCIRC)*, pp. 14-17, Sept. 2012.

7. Kyoungtae Lee, Yeonam Yoon, and **Nan Sun**, "A 10MHz-BW, 5.6mW, 70dB SNDR delta-sigma ADC using VCO-based integrators with intrinsic DEM," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2006-2009, May 2013.

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8. Wenjuan Guo, Youngchun Kim, Arindam Sanyal, Ahmed Tewfik, and **Nan Sun**, "A single SAR ADC converting multi-channel sparse signals," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2235-2238, May 2013.
9. Travis Forbes, Wei-Gi Ho, **Nan Sun**, and Ranjit Gharpurey, "A frequency-folded ADC architecture with digital LO synthesis," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 149-152, May 2013.
10. Arindam Sanyal and **Nan Sun**, "A very high energy-efficiency switching technique for SAR ADCs," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 229-232, Aug. 2013.
11. Rohit Yadav and **Nan Sun**, "A 1.2mW 67.5 dB SQDR VCO-based sigma delta ADC with non-linearity cancellation technique," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 570-573, Aug. 2013.
12. Long Chen, Manzur Rahman, Sha Liu, and **Nan Sun**, "A fast radix-3 SAR analog-to-digital converter," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1148-1151, Aug. 2013.
13. Kyoungtae Lee, Yeonam Yoon, and Nan Sun, "A 1.8mW 2MHz-BW 66.5dB-SNDR delta-sigma ADC using VCO-based integrators with intrinsic CLA," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-4, Sept. 2013.
14. Arindam Sanyal and **Nan Sun**, "A low frequency-dependence, energy-efficient switching technique for bottom-plate sampled SAR ADC," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 297-300, June 2014.
15. Xiankun Jin and **Nan Sun**, "Low-cost high-quality constant offset injection for SEIR-based ADC built-in-self-test," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 285-288, June 2014.
16. Peijun Wang and **Nan Sun**, "A random DEM technique with minimal element transition rate for high-speed DACs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1155-1158, June 2014.
17. Long Chen, Ji Ma, and **Nan Sun**, "Capacitor mismatch calibration for SAR ADCs based on comparator metastability detection," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2357-2360, June 2014.
18. Arindam Sanyal and **Nan Sun**, "An enhanced ISI shaping technique for multi-bit delta sigma DACs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2341-2344, June 2014.
19. Yeonam Yoon, Kyoungtae Lee, Peijun Wang, and **Nan Sun**, "A purely-VCO-based single-loop high-order continuous-time delta sigma ADC," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 926-929, June 2014.
20. Manzur Rahman, Long Chen, and **Nan Sun**, "Algorithm and implementation of digital calibration of fast converging radix-3 SAR ADC," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1336-1339, June 2014.
21. K. R. Raghunandan, **Nan Sun**, and T.R. Viswanathan, "Analog signal processing in deep submicron CMOS technologies using inverters, " *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 394-397, Aug. 2014.
22. Arindam Sanyal, Kareem Ragab, Long Chen, T.R. Viswanathan, Shouli Yan, and **Nan Sun**, "A hybrid SAR-VCO delta-sigma ADC with first-order noise shaping," *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2014.
23. Long Chen, Arindam Sanyal, Ji Ma, and **Nan Sun**, "A 24-uW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique," *European Solid-State Circuit Conference (ESSCIRC)*, pp. 219-222, Sept. 2014.
24. Nicholas Wood and **Nan Sun**, "Predicting ADC - a new approach to low power ADC design," *IEEE Dallas Circuits and Systems Conference (DCAS)*, pp. 1-4, Oct. 2014.
25. Wenjuan Guo, Youngchun Kim, Ahmed Tewfik, and **Nan Sun**, "Ultra-low power multi-channel data conversion with a single SAR ADC for mobile sensing applications", *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2015.
26. Yeonam Yoon, Koungtae Lee, Sungjin Hong, Xiyuan Tang, Long Chen, and **Nan Sun**, "A 0.04-mm2 0.9-mW 71-dB SNDR distributed modular ΔΣ ADC with VCO-based integrator and digital DAC calibration," *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2015.
27. Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and **Nan Sun**, "A 10.5-b ENOB 645nW 100kS/s SAR ADC with statistical estimation based noise reduction," *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2015.
28. Kareem Ragab and **Nan Sun**, "A 12b ENOB, 2.5MHz-BW, 4.8mW VCO-based 0-1 MASH ADC with direct digital background nonlinearity calibration," *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2015.

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29. Long Chen, Arindam Sanyal, Ji Ma, Xiyuan Tang, and **Nan Sun,** "Comparator common-mode variation effects analysis and its application in SAR ADCs," *IEEE International Symposium on Circuits and Systems*, accepted.
30. Arindam Sanyal and **Nan Sun,** "A 18.5-fJ/step VCO-based 0-1 MASH delta-sigma ADC with digital background calibration," *IEEE Symposium on VLSI Circuits*, pp. 26-27, Jun. 2016.
31. Wenjuan Guo and **Nan Sun,** "A 9.8b-ENOB 5.5fJ/step fully-passive compressive sensing SAR ADC for WSN applications," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 91-94, Sept. 2016.
32. Shaolan Li and **Nan Sun,** "A 174.3dB FoM VCO-based CT $\Delta\Sigma$ modulator with a fully digital phase extended quantizer and tri-level resistor DAC in 130nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 241-244, Sept. 2016.
33. Kareem Ragab and **Nan Sun,** "A 1.4mW 8b 350MS/s loop-unrolled SAR ADC with background offset calibration in 40nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 417-420, Sept. 2016.
34. Arindam Sanyal and **Nan Sun,** "A 55fJ/conv-step hybrid SAR-VCO delta sigma capacitance-to-digital converter in 40nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 385-388, Sept. 2016.
35. Xiyuan Tang, Long Chen, Jeonggoo Song, and **Nan Sun,** "A 10-b 750µW 200MS/s fully dynamic single-channel SAR ADC in 40nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 413-416, Sept. 2016.
36. Wenjuan Guo and **Nan Sun,** "A 12b-ENOB 61µW noise-shaping SAR ADC with a passive integrator," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 405-408, Sept. 2016.
37. Jeonggoo Song, Kareem Ragab, Xiyuan Tang, and **Nan Sun,** "A 10-b 800MS/s time-interleaved SAR ADC with fast timing-skew calibration," *IEEE Asian Solid-State Circuits Conference (ASSCC)*, accepted.

C.   Chapters of Books

1. **Nan Sun** and Donhee Ham, "Chapter 6: Hardware Developments, Handheld NMR systems for biomolecular sensing," invited book chapter in *Mobile NMR and MRI*, Royal Society of Chemistry (Edited by Michael Johns), pp. 158-182, 2015.
2. **Nan Sun** and Donhee Ham, "Handheld NMR systems and their applications for biomolecular sensing," invited book chapter in *Point of Care Diagnostics on a Chip*, Springer (Edited by Robert Westervelt and David Issadore), pp. 177-196, 2012.
3. Ozgur Yildirim, **Nan Sun**, and Xiaofeng Li, "Chaotic soliton oscillator and communications," invited book chapter in *Electrical Solitons: Theory, Design, and Applications*, CRC press, pp. 197-208, 2012.
4. **Nan Sun**, Yong Liu, and Donhee Ham, "Low cost diagnostics – RF designer's approach," invited book chapter in *CMOS Biosystems: Where Electronics Meets Biology*, Wiley (Edited by Kris Iniewski), pp. 1629-1643, 2011.

ORAL PRESENTATIONS:

1. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Cirrus Logic, TX, 6/2016.
2. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Stanford University, CA, 5/2016.
3. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Intel Labs, OR, 5/2016.
4. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Oregon State University, Corvallis, OR, 5/2016.
5. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," University of Southern California, Los Angeles, CA, 4/2016.
6. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," University of California at Los Angeles, Los Angeles, CA, 4/2016.
7. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Broadcom Ltd, Irvine, CA, 4/2016.
8. **Nan Sun,** "Low power analog and mixed-signal IC design for bio-signal detection," BioWireless, Austin, TX, 1/2016.
9. **Nan Sun,** "Advanced analog IC design techniques," Tsinghua University, Beijing, China, 11/2015.
10. **Nan Sun,** "Advanced dynamic element matching techniques for both static and dynamic errors in CT $\Delta\Sigma$ modulator," Cirrus Logic, TX, 6/2015.
11. **Nan Sun,** "Handheld CMOS NMR biosensor," Case Western Reserve University, Cleveland, OH, 4/2015.

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12. **Nan Sun,** "Scaling-friendly VCO-based $\Delta\Sigma$ ADC design in advanced CMOS processes," Texas A&M University, College Station, TX, 4/2015.
13. **Nan Sun,** "Low power SAR ADC and high-speed background timing skew calibration," Silicon Labs, Austin, TX, 10/2014.
14. **Nan Sun,** "High performance SAR ADC design," Beijing Microelectronic Technology Institute, 8/2014.
15. **Nan Sun,** "Low-power SAR ADC design," Cirrus Logic, Austin, TX, 6/2014.
16. **Nan Sun,** "Advanced analog IC research," TSMC, Austin, TX, 5/2014.
17. **Nan Sun,** "Handheld CMOS NMR biosensor," Texas Tech University, Lubbock, TX, 11/2013.
18. **Nan Sun,** "Scaling-friendly VCO-based $\Delta\Sigma$ ADC design in advanced CMOS processes," Cirrus Logic, Austin, TX, 11/2013.
19. **Nan Sun,** "Scaling-friendly VCO-based $\Delta\Sigma$ ADC design in advanced CMOS processes," Freescale, AZ, 9/2013.
20. **Nan Sun,** "Handheld CMOS NMR biosensor," Texas Instruments at Santa Clara, CA, 7/2013.
21. **Nan Sun,** "Handheld CMOS NMR biosensor," Kilby Lab, Texas Instruments, TX, 7/2013.
22. **Nan Sun,** "Handheld CMOS NMR biosensor," Texas Instruments, TX, 1/2013.
23. **Nan Sun,** "Mismatch shaping techniques for multibit $\Delta\Sigma$ ADCs," Cirrus Logic, Austin, TX, 1/2013.
24. **Nan Sun,** "Handheld CMOS NMR biosensor," Samsung Research, Dallas, TX, 12/2012.
25. **Nan Sun,** "Advanced dynamic element matching techniques," Synaptics, Austin, TX, 12/2012.
26. **Nan Sun,** "Advanced dynamic element matching techniques," Texas Instruments, TX, 11/2012.
27. **Nan Sun,** "Handheld CMOS NMR biosensor," IEEE Instrumentation and Measurement Chapter, Austin, TX, 05/21/2012.
28. **Nan Sun,** "Handheld CMOS NMR biosensor," Qualcomm, San Diego, CA, 04/13/2012.
29. **Nan Sun,** "Handheld CMOS NMR biosensor," Intel, Portland, OR, 02/17/2012.
30. **Nan Sun,** "Handheld CMOS NMR biosensor," Peking University, Beijing, China, 01/05/2012.
31. **Nan Sun,** "Handheld CMOS NMR biosensor," RWTH Aachen University, Aachen, Germany, 12/13/2011.
32. **Nan Sun,** "Handheld CMOS NMR biosensor," University of Texas at Dallas, Dallas, TX, 11/11/2011.
33. **Nan Sun,** "Handheld CMOS NMR biosensor," IEEE SSCS/CAS Austin Chapter, Austin, TX, 11/02/2011.
34. **Nan Sun,** "Handheld CMOS NMR biosensor," Silicon Labs, Austin, TX, 09/16/2011.
35. **Nan Sun,** "Handheld CMOS NMR biosensor," ICMRM 11, Beijing, China, 08/16/2011.
36. **Nan Sun,** "Handheld CMOS NMR systems," Halliburton, Houston, TX, 06/24/2011.
37. **Nan Sun,** "Advanced dynamic element matching techniques," Tsinghua University, Beijing, China, 01/04/2011.
38. **Nan Sun,** "Handheld CMOS NMR biosensor," IBM T. J. Watson Research Center, Yorktown Heights, NY, 12/10/2010.
39. **Nan Sun,** "Handheld CMOS NMR biosensor," Bruker Biospin Inc., Billerica, MA, 11/16/2010.
40. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, 07/09/2010.
41. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Tsinghua University, Beijing, China, 07/05/2010.
42. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Institute of Electronics, Chinese Academy of Sciences, Beijing, China, 07/01/2010.
43. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Fudan University, Shanghai, China, 06/17/2010.
44. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Shanghai Jiaotong University, Shanghai, China, 06/17/2010.
45. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Rice University, Houston, TX, 04/14/2010.
46. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Stanford University, Stanford, CA, 04/08/2010.
47. **Nan Sun,** "Handheld CMOS NMR biosensor," University of Texas at Austin, Austin, TX, 03/25/2010.
48. **Nan Sun,** "Handheld CMOS NMR biosensor," Harvard University, Cambridge, MA, 03/22/2010.
49. **Nan Sun,** "Handheld CMOS NMR biosensor," Schlumberger-Doll Research Center, Cambridge, MA, 03/10/2010.
50. **Nan Sun,** "Handheld CMOS NMR biosensor," Stanford University, Stanford, CA, 02/04/2010.
51. **Nan Sun,** "CMOS NMR biosensor," Harvard University, 02/02/2010.

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52. **Nan Sun,** "CMOS NMR biosensor," CMOS Emerging Technology Conference, Calgary, Canada, 02/2009.

PATENTS:

1. **Nan Sun**, Yong Liu, Hakho Lee, Ralph Weisselder, and Donhee Ham, "Miniaturized magnetic resonance systems and methods," US patent application number 12/681,303.
2. **Nan Sun** and Donhee Ham, "Systems and methods for design and construction of NMR transceiver circuits," US patent application number 12/919,215.
3. **Nan Sun**, "Dual-mode-based digital background calibration for gain variations and device mismatches," US patent application number 12/649,274.
4. Long Chen, Xiyuan Tang, and **Nan Sun**, "Statistical estimation based noise reduction technique for low power successive approximation register analog-to-digital converter," US patent application number 62/233,683 (pending).
5. Wenjuan Guo and **Nan Sun**, "Low-power passive noise-shaping SAR," US application number 62/250,709 (pending).
6. **Nan Sun**, "Fractional-N phase lock loop apparatus and method using multi-element fractional dividers," US patent application number 62/308,528 (pending).

GRANTS AND CONTRACTS: Total funding ≈ \$3.4M (my share ≈ \$1.7M)

Co-Investigators	Title	Agency	Project Total	Candidate's Share	Grant Period
PI: NS. David Pan (co-PI)	SHF: Small: Design/Automation for Synthesizable and Scaling Friendly Analog/Mixed-Signal Circuits	NSF	\$450K	\$225K	2015-2018
PI: Nanshu Lu (Aerospace); co-PI: Nan Sun	Stretchable Planar Antenna Modulated by Integrated Circuit (SPAMIC) for the Near Field Communication (NFC) of Epidermal Electrophysiological Sensors (EEPS)	NSF	\$380K	\$190K	2015-2018
Sub-award PI: Nanshu Lu (Aerospace); Sub-award co-PI: Nan Sun; PI: Katherine Steele (University of Washington)	Ubiquitous rehabilitation to monitor and improve muscle activity and movement after neurologic injury	NIH	\$1.5M total, \$370K sub-award total	\$185K	2015-2019
PI: Nan Sun	CAREER: Combining nuclear magnetic resonance with IC technology	NSF	\$400K	\$400K	2013-2018
PI: Nan Sun	High temperature LNA design	China Oil-Service Ltd	\$75K	\$75K	2015
PI: Nan Sun	Low-power high-speed ADC for CMOS image sensor	Samsung	\$100K	\$100K	2015
PI: Nan Sun	Multichannel MRI transceiver design	Samsung	\$100K	\$100K	2014
PI: Nan Sun	Miniature NMR systems	Formation	\$105K	\$105K	2011-2014

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	for rock and outcrop analysis	Evaluation Industry Consortium			
PI: Nan Sun	Student design contest	Texas Instruments	$20K	$20K	2011-2015
PI: Nan Sun	Gift	Texas Instruments	$60K	$60K	2015
PI: Nan Sun	Gift	Texas Instruments	$60K	$60K	2014
PI: Nan Sun	Gift	Texas Instruments	$60K	$60K	2013
PI: Nan Sun	Gift	Cirrus Logic	$20K	$20K	2016
PI: Nan Sun	Gift	Cirrus Logic	$20K	$20K	2014
PI: Nan Sun	Gift	Cirrus Logic	$20K	$20K	2013
PI: Nan Sun	Gift	Cirrus Logic	$20K	$20K	2012
PI: Nan Sun	Gift	Intel	$18K	$18K	2012
PI: Nan Sun	Gift	Intel	$30K	$30K	2011
Total			**$3.4M**	**$1.7M**	

EXTERNAL IN-KIND DONATIONS (Total market value ≈ $0.7M; my share ≈ 0.5M)

	Free Integrated Circuit (IC) Fabrication	**Company**	**Donation in Value**	**Candidate's Share**	**Year**
Lead PI	4 mm^2 free IC fabrication in 130nm	MOSIS	$20K	$10K	2016
Lead PI	Twice 9 mm^2 free IC fabrication in 40nm	TSMC	$180K	$180K	2016
Lead PI	Twice 25 mm^2 free IC fabrication in 180nm	TSMC	$60K	$60K	2016
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	$37.5K	2015
Lead PI	Twice 9 mm^2 free IC fabrication in 40nm	TSMC	$90K	$90K	2015
Lead PI	25 mm^2 free IC fabrication in 180nm	TSMC	$30K	$30K	2015
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	$37.5K	2015
Single PI	1 mm^2 free IC fabrication in 65nm	Texas Instruments	$10K	$10K	2014
Single PI	1 mm^2 free IC fabrication in 65nm	Samsung	$10K	$10K	2014
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	$37.5K	2014
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	$37.5K	2013
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	$37.5K	2012
Total			**$0.7M**	**$0.5M**	

PH.D. SUPERVISIONS COMPLETED:

Name	**Year**	**Thesis Title**	**Department**	**Co-Supervisor**	**University**
Arindam Sanyal	2015	Digital Enhancement Techniques for Data Converters In Scaled CMOS Technologies	ECE		UT Austin
Wenjuan Guo	2016	Fully-Passive Switched-Capacitor Techniques for High Performance SAR ADC Design	ECE		UT Austin
Long Chen	2016	Design Techniques for Low-power SAR ADCs in Nano-scale CMOS	ECE		UT Austin

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Name	Year	Thesis or Report Title	Department	Co-Supervisor	University
		Technologies			
Kareem Ragab	2016	Background Calibration Techniques For Analog-to-Digital Converters In Scaled CMOS Technologies	ECE	Michael Orshansky	UT Austin

M.S. SUPERVISIONS COMPLETED:

Name	Year	Thesis or Report Title	Department	Co-Supervisor	University
Marco Moreno	2012	An Android Hosted Bluetooth EKG Monitoring Device	ECE		UT Austin
Harold Bautista	2012	Performance Analysis of Different Voltage Controlled Delay Lines in a Delay-Locked Loop	ECE		UT Austin
Miguel Gandara	2012	A 12-bit, 10 MS/s Two Stage SAR-Based Pipeline ADC	ECE		UT Austin
Alex Fontaine	2013	Investigation of 10-Bit SAR ADC Using Flip-Flip Bypass Circuit	ECE		UT Austin
Shitong Zhao	2013	Not applicable	ECE		UT Austin
Xiankun Jin	2013	A SEIR-Based ADC Built-In-Self-Test and Its Application in ADC Self-Calibration	ECE		UT Austin
Olga Kardonik	2013	A Study of SAR ADC and Implementation of 10-bit Asynchronous Design	ECE		UT Austin
Kyoungtae Lee	2014	Design of Low-power Area-efficient Continuous-time $\Delta\Sigma$ ADC Using VCO-Based Integrators with Intrinsic CLA	ECE		UT Austin
Ji Ma	2014	A Study of Capacitor Array Calibration for a Successive Approximation Analog-to-Digital Converter	ECE		UT Austin
You Li	2015	Design and Implementation on High-order Mismatch-shaped Multibit Delta-Sigma D/A Converters	ECE		UT Austin
Anoosh Gnana	2015	Pseudo Pipelined SAR ADC with Regenerative Amplifier	ECE		UT Austin
Phillippe Dollo	2016	System-Level Design and Analysis of an Embedded Audio Signal Processing Application	ECE		UT Austin
Paridhi Gulati	2016	A 10MS/s Pipelined ADC with a First Stage Conventional SAR ADC Followed by a Multi-bit Per Cycle SAR ADC	ECE		UT Austin
Sowmya Katragadda	2016	Noise Shaping Asynchronous SAR ADC Based Time to Digital Converter	ECE		UT Austin

PH.D. IN PROGRESS:

| Student	Degree	Status	Start Date	Completion
Yeonam Yoon	Ph.D.	In Candidacy	Fall 2011	Spring 2017 (est.)
Raghunadan Raghunathan	Ph.D.	In Candidacy	Fall 2011	Spring 2017 (est.)
Manzur Rahman	Ph.D.	In Candidacy	Fall 2012	Spring 2017 (est.)

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Electrical and Computer Engineering   Revised September 29, 2016

Mikel Ash	Ph.D.	Pre-candidacy	Fall 2012	Fall 2017 (est.)
Shaolan Li	Ph.D.	Pre-candidacy	Fall 2012	Fall 2017 (est.)
Songjin Hong	Ph.D.	Pre-candidacy	Fall 2012	Fall 2017 (est.)
Miguel Gandara	Ph.D.	Pre-candidacy	Fall 2012	Fall 2017 (est.)
Xiyuan Tang	Ph.D.	Pre-candidacy	Fall 2012	Spring 2018 (est.)
Jeonggoo Song	Ph.D.	Pre-candidacy	Fall 2013	Spring 2018 (est.)
Linxiao Shen	Ph.D.	Pre-candidacy	Fall 2014	Spring 2019 (est.)
Abhishek Mukerjee	Ph.D.	Pre-candidacy	Fall 2014	Spring 2019 (est.)

M.S. IN PROGRESS:

Student	Degree	Status	Start Date	Completion
Jiawen Fu	M.S.	1st-year	Fall 2015	Spring 2017 (est.)
Chang Liu	M.S.	1st-year	Fall 2015	Spring 2017 (est.)

VITA:
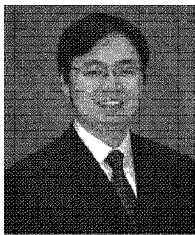
Nan Sun is Assistant Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin. He received the B.S. degree from Tsinghua University, Beijing, China in 2006, where he ranked top in Department of Electronic Engineering. He received the Ph.D. degree from the School of Engineering and Applied Sciences at Harvard University in 2010.

Dr. Sun is a Fellow of the AMD Chair in Computer Engineering at UT Austin. He received NSF Career Award in 2013 and Jack Kilby Research Award from UT Austin in 2015. He also received Samsung Fellowship, Hewlett Packard Fellowship, and Analog Devices Outstanding Student Designer Award in 2003, 2006, and 2007, respectively. He won Harvard Teaching Award in three consecutive years: 2008, 2009, and 2010. He serves in the technical program committee of *Custom Integrated Circuits Conference* and *Asian Solid-State Circuit Conference*. He is Associate Editor for *IEEE Transactions on Circuits and Systems – I, Regular Papers*.

His research interests include: 1) analog, mixed-signal, and RF integrated circuits; 2) miniature spin resonance systems; 3) magnetic sensors and image sensors; 4) developing micro- and nano-scale solid-state platforms (silicon ICs and beyond) to analyze biological systems for biotechnology and medicine.

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Master Promotion Summary Table
Nan Sun

Metric	Value
Peer-reviewed journal publications (in rank **and total**)	23 / 27
Peer-reviewed conference proceedings (in rank **and total**)	34 / 37
Number of **journal** papers **in rank** with UT students **as co-authors**	15
Total citations of all publications (career) **from ISI Web of Knowledge**	228
h-index (career) **from ISI Web of Knowledge** *	7
Total citations of all publications (career) **from Google Scholar or Publish or Perish**	489
h-index (career) **from Google Scholar or Publish or Perish** *	12
Total external research funding raised	$3.4M
Total external research funding raised (candidate's share)	$1.7M
Total number of external grants/contracts **awarded**	18
Number of external grants/contracts **awarded** as PI	16
PhD students completed†	3.5 (3 sole advisor)
MS students completed†	14 (14 sole advisor)
PhD students in pipeline (as of 09/2016) †	10 (9 sole advisor)
MS students in pipeline (as of 09/2016) †	2 (2 sole advisor)
Number of courses taught	8
Total # of students taught in organized courses	256
Average instructor evaluation for UG courses	4.55
Average instructor evaluation for Grad courses	4.83
Average course evaluation for UG courses	4.30
Average course evaluation for Grad courses	4.65
Teaching awards	0
Student organizations advised	0
Undergraduate **researchers** supervised	6
Service on journal editorial boards	2
Number of symposia organized	5

Provide a printout/screen shot of the first page of the report from both ISI Web of Knowledge and Google Scholar

† Count a student as 1.0 if sole supervisor and 0.5 if co-supervised.

Complete Reverse Chronological List of Publications and Scholarly/Creative Works

Nan Sun
Electrical and Computer Engineering
The University of Texas at Austin
nansun@mail.utexas.edu

Title of Dissertation: Handheld CMOS NMR Systems and Their Applications for Biomedical Sensing
Dissertation Advisor: Donhee Ham, Harvard University

SECTION 1: WORKS PUBLISHED IN PRESS, ACCEPTED, OR UNDER CONTRACT WHILE IN CURRENT RANK AT UT AUSTIN

PUBLISHED OR ACCEPTED JOURNAL PAPERS

Kareem Ragab and **Nan Sun**, "A 12b ENOB, 2.5MHz, 4.8mW VCO-based 0-1 MASH with direct digital background calibration," accepted to *IEEE Journal of Solid-State Circuits*.

- Co-authors: Kareem Ragab is my PhD student.
- Qualitative statement of contribution: My student and I together came up with the original idea. I worked with my student to finish the prototype chip design and testing. I advised him on the paper writing.

Arindam Sanyal and **Nan Sun**, "A second-order VCO-based delta sigma ADC using a modified DPLL," *Electronics Letters*, vol. 52, no. 14, accepted.

- Co-authors: Arindam Sanyal is my PhD student.
- Qualitative statement of contribution: The student performed the majority of the work. He came up with the original idea. I offered technical feedback and advised him on the paper writing.

Long Chen, Kareem Ragab, Xiyuan Tang, Jeonggoo Song, Arindam Sanyal, and **Nan Sun**, "A 0.95-mW 6-b 700-Ms/s single-channel loop-unrolled SAR ADC in 40-nm CMOS," *IEEE Transactions on Circuits and Systems - II*, accepted.

- Co-authors: Long, Kareem, Xiyuan, Jeonggoo, and Arindam are all my PhD students.
- Qualitative statement of contribution: I came up with the original idea. I worked with my students to finish the prototype chip design and testing. I advised them on paper writing.

Arindam Sanyal, Xueyi Yu, Yanlong Zhang, and **Nan Sun**, "Fractional-N PLL with Multi-Element Fractional Divider for Noise Reduction," *Electronic Letters*, vol. 52, no. 10, pp. 809-810, May 2016.

- Co-authors: Arindam is my PhD student. Yanlong is my visiting PhD student. Xueyi is a design manager at Spintrol Ltd.
- Qualitative statement of contribution: I came up with the original idea. I advised my students to complete the architectural level circuit design and simulation, as well as the paper writing.

Kyoungtae Lee, Yeonam Yoon, and **Nan Sun**, "A scaling-friendly low-power small-area delta-sigma ADC with VCO-based integrator and intrinsic mismatch shaping capability," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 561-573, Dec. 2015.

- Co-authors: Kyoungtae is my Master's student. Yeonam is my PhD student.
- Qualitative statement of contribution: I came up with the original idea. I worked with my students to finish the prototype chip design and testing. I advised them on paper writing.

Arindam Sanyal and **Nan Sun**, "Dynamic element matching techniques for static and dynamic errors in continuous-time multi-bit delta-sigma modulators," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 598-611, Dec. 2015.

- Co-authors: Arindam is my PhD student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student to complete the architectural level circuit design and simulation, as well as the paper writing.

Arindam Sanyal, Long Chen, and **Nan Sun**, "Dynamic element matching with signal-independent element transition rates for multibit delta sigma modulators," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 62, no. 5, pp. 1325-1334, May, 2015.

- Co-authors: Arindam and Long are my PhD students.
- Qualitative statement of contribution: I came up with the original idea. I advised my student to complete the architectural level circuit design and simulation, as well as the paper writing.

Dongwan Ha, **Nan Sun**, and Donhee Ham, "Next generation multi-dimensional NMR spectrometer based on semiconductor technology," *eMagRes*, vol. 4, pp. 117-125, 2015.

- Co-authors: Donhee is my PhD advisor. Dongwan is Donhee's PhD student.
- Qualitative statement of contribution: This is an invited review paper. I contributed to the paper writing.

Wenjuan Guo, Tsedeniya Abraham, Steven Chiang, Chintan Trehan, Masahiro Yoshioka, and **Nan Sun**, "An area and power-efficient Iref compensation technique for voltage-mode R-2R DACs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 62, no. 7, pp. 656-660, July 2015.

- Co-authors: Wenjuan is my PhD student. Tsedeniya, Steven, Chintan, Masahiro are with

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Texas Instruments.
- Qualitative statement of contribution: My PhD student came up with the original idea. I advised her on the idea development, overall circuit design, and paper writing.

Manzur Rahman, Arindam Sanyal, and **Nan Sun**, "A novel hybrid radix-3/radix-2 SAR ADC with fast convergence and low hardware complexity," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 62, no. 5, pp. 426-430, May 2015.

- Co-authors: Manzur and Arindam are my PhD students.
- Qualitative statement of contribution: I came up with the original idea. I advised my student to complete the architectural level circuit design and simulation, as well as the paper writing.

Kareem Ragab, Long Chen, Arindam Sanyal, and **Nan Sun**, "Digital background calibration for pipelined ADCs based on comparator decision time quantization," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 62, no. 5, pp. 456-460, May 2015.

- Co-authors: Kareem, Long, and Arindam are my PhD students.
- Qualitative statement of contribution: I came up with the original idea. I advised my students on detailed theoretical analysis, circuit design, and paper writing.

Dongwan Ha, Jeffrey Paulsen, **Nan Sun**, Yi-Qiao Song, and Donhee Ham, "Scalable NMR spectroscopy with semiconductor chips," *Proceedings of National Academy of Engineering (PNAS)*, vol. 111, no. 33, pp. 11955–11960, Aug. 2014.

- Co-authors: Donhee is my PhD adviser. Dongwan is Donhee's PhD student. Jeffrey and Yi-Qiao are with Schlumberger Ltd.
- Qualitative statement of contribution: I contributed to the design of the circuits and the paper writing.

Arindam Sanyal, Peijun Wang, and **Nan Sun**, "A thermometer-like mismatch shaping technique with minimum element transition activity for multi-bit delta-sigma DACs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 61, no. 7, pp. 461-465, Jul. 2014.

- Co-authors: Arindam is my PhD student. Peijun is my Master's student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student to complete the architectural level circuit design and simulation, as well as the paper writing.

Arindam Sanyal and **Nan Sun**, "An energy-efficient, low frequency-dependence switching technique for SAR ADCs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 61, no. 5, pp. 294-298, May 2014.

- Co-authors: Arindam is my PhD student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the overall circuit and the paper writing.

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Arindam Sanyal and **Nan Sun**, "SAR ADC architecture with 98% reduction in switching energy over conventional scheme," *Electronics Letters*, vol. 49, pp. 248-250, 2013.

- Co-authors: Arindam is my PhD student.
- Qualitative statement of contribution: The student came up with the original idea. I offered technical feedback and advised him on the paper writing.

Kareem Ragab, Mucahit Kozak, and **Nan Sun**, "Thermal noise analysis of a programmable-gain switched-capacitor amplifier with input offset cancellation," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 60, pp. 147-151, Mar. 2013.

- Co-authors: Kareem is my PhD student. Mucahit is with Synaptics Inc.
- Qualitative statement of contribution: My PhD student came up with the original theoretical analysis. I offered technical feedback and guided my student on the paper writing.

Nan Sun, Yong Liu, Ling Qin, Hakho Lee, Ralph Weissleder, and Donhee Ham, "Small NMR biomolecular sensor," *Journal of Solid-State Electronics* (invited paper), 2013.

- Co-authors: Donhee is my PhD advisor. Yong is Donhee's PhD student. Hakho and Ralph are professors at Harvard Medical School.
- Qualitative statement of contribution: This is an invited review paper. I wrote the majority of this paper.

Youngchun Kim, Wenjuan Guo, Vikrham Gowreesunker, **Nan Sun**, and Ahmed Tewfik, "Multi-channel sparse data conversion with a single analog-to-digital converter," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 2, pp. 470-481, Sept. 2012.

- Co-authors: Wenjuan is my PhD student. Ahmed is a Professor in the ECE Dept. at UT Austin, Youngchun and Vikrham are Ahmed's PhD students.
- Qualitative statement of contribution: I designed the majority of the circuits. I offered technical feedback to Youngchun and Wenjuan. I also advised students on the paper writing.

Nan Sun, "Exploiting process variation and noise to calibration gain nonlinearities in pipelined ADCs," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 4, pp. 685-695, Apr. 2012.

- Co-authors: None.
- Qualitative statement of contribution: I came up with the original idea, and finished all the analysis, modeling, validation, and paper writing.

Nan Sun, "High-order mismatch-shaped segmented multibit delta-sigma DACs with arbitrary unit weights," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 2, pp. 295-304, Feb. 2012.

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- Co-authors: None.
- Qualitative statement of contribution: I came up with the original idea, and finished all the analysis, modeling, validation, and paper writing.

Nan Sun and Peiyan Cao, "Low-complexity high-order vector-based mismatch shaping in multi-bit $\Delta\Sigma$ ADCs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 58, no. 12, pp 872-876, Dec. 2011.

- Co-authors: Peiyan was a graduate student at Cornell University.
- Qualitative statement of contribution: I came up with original idea, and finished the majority of the circuit analysis, modeling, validation, and paper writing.

Nan Sun, "High-order mismatch-shaping in multibit DACs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 58, no. 6, pp 346-350, Jun. 2011.

- Co-authors: None
- Qualitative statement of contribution: I came up with the original idea, and finished all the analysis, modeling, validation, and paper writing.

Nan Sun, Tae-Jong Yoon, Hakho Lee, William Andress, Ralph Weissleder, and Donhee Ham, "Palm NMR and one-chip NMR," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 342-352, Jan. 2011.

- Co-authors: Tae-Jong is post-doc at Harvard Medical School, Hakho and Ralph are faculty at Harvard Medical School, Donhee is my PhD advisor, William is Donhee's PhD student.
- Qualitative statement of contribution: This paper is mainly based on my PhD work. I came up with the original idea. I constructed the entire hardware system and performed the majority of the experiments. I also wrote the majority of the paper.

PUBLISHED OR ACCEPTED COMPETITIVE CONFERENCE PAPERS

Jeonggoo Song, Kareem Ragab, Xiyuan Tang, and Nan Sun, "A 10-b 800MS/s time-interleaved SAR ADC with fast timing-skew calibration," *IEEE Asian Solid-State Circuits Conference (ASSCC)*, accepted.

- Co-authors: Jeonggoo, Kareem, and Xiyuan are my PhD students.
- Qualitative statement of contribution: I came up with original idea. I advised my student on the circuit design, simulation, validation, and testing. I also guided my student on the paper writing.

Wenjuan Guo and **Nan Sun**, "A 12b-ENOB 61μW Noise-Shaping SAR ADC with a Passive Integrator," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, accepted.

- Co-authors: Wenjuan is my PhD student.

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- Qualitative statement of contribution: I came up with original idea. I advised my student on the circuit design, simulation, validation, and testing. I also guided my student on the paper writing.

Wenjuan Guo and **Nan Sun**, "A 9.8b-ENOB 5.5fJ/Step Fully-Passive Compressive Sensing SAR ADC for WSN Applications," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, accepted.

- Co-authors: Wenjuan is my PhD student.
- Qualitative statement of contribution: The student came up with the original idea. I advised my student on the idea development, the circuit design, simulation, validation, and testing. I also guided my student on the paper writing.

Shaolan Li and **Nan Sun**, "A 174.3dB FoM VCO-Based CT $\Delta\Sigma$ Modulator with a Fully Digital Phase Extended Quantizer and Tri-Level Resistor DAC in 130nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, accepted.

- Co-authors: Shaolan is my PhD student.
- Qualitative statement of contribution: I came up with the basic idea. I advised my student on the circuit analysis, design, simulation, validation, and testing. I also guided my student on the paper writing.

Kareem Ragab and **Nan Sun**, "A 1.4mW 8b 350MS/s Loop-Unrolled SAR ADC with Background Offset Calibration in 40nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, accepted.

- Co-authors: Kareem is my PhD student.
- Qualitative statement of contribution: The student came up with the original idea. I advised my student on the circuit analysis, design, simulation, validation, and testing. I also guided my student on the paper writing.

Arindam Sanyal and **Nan Sun**, "A 55fJ/conv-step Hybrid SAR-VCO Delta Sigma Capacitance-to-Digital Converter in 40nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, accepted.

- Co-authors: Arindam is my PhD student.
- Qualitative statement of contribution: I came up with the basic idea. I advised my student on the circuit analysis, design, simulation, validation, and testing. I also guided my student on the paper writing.

Xiyuan Tang, Long Chen, Jeonggoo Song, and **Nan Sun**, "A 10-b 750µW 200MS/s Fully Dynamic Single-Channel SAR ADC in 40nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, accepted.

- Co-authors: Xiyuan, Long, and Jeonggoo are all my PhD students.
- Qualitative statement of contribution: I came up with the original idea. I advised my

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student on the circuit analysis, design, simulation, validation, and testing. I also guided my student on the paper writing.

Long Chen, Arindam Sanyal, Ji Ma, Xiyuan Tang, and **Nan Sun,** "Comparator Common-Mode Variation Effects Analysis and its Application in SAR ADCs," *IEEE International Symposium on Circuits and Systems,* accepted.

- Co-authors: Long, Arindam, and Xiyuan are my PhD students. Ji is my Master's student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Arindam Sanyal and **Nan Sun,** "A 18.5-fJ/step VCO-Based 0-1 MASH Delta-Sigma ADC with Digital Background Calibration," *IEEE Symposium on VLSI Circuits,* pp. 26-27, Jun. 2016.

- Co-authors: Arindam is my PhD student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis, design, simulation, validation, and testing. I also guided my student on the paper writing.

Wenjuan Guo, Youngchun Kim, Ahmed Tewfik, and **Nan Sun,** "Ultra-Low Power Multi-channel Data Conversion with a Single SAR ADC for Mobile Sensing Applications", *Custom Integrated Circuit Conference (CICC),* pp. 1-4, Sept. 2015.

- Co-authors: Wenjuan is my PhD student. Ahmed is a Professor in the ECE Dept. at UT Austin. Youngchun is Ahmed's PhD student.
- Qualitative statement of contribution: My student came up with original idea. I advised my student on the circuit analysis, design, simulation, validation, and testing. I also guided my student on the paper writing.

Yeonam Yoon, Kyoungtae Lee, Sungjin Hong, Xiyuan Tang, Long Chen, and **Nan Sun,** "A 0.04-mm2 Modular ΔΣ ADC with VCO-based Integrator and 0.9-mW 71-dB SNDR Distributed Digital DAC Calibration", *Custom Integrated Circuit Conference (CICC),* pp. 1-4, Sept. 2015.

- Co-authors: Yeonam, Sungjin, Xiyuan, and Long are my PhD students. Kyoungtae is my Master's student.
- Qualitative statement of contribution: I came up with the original idea. I advised my students on the circuit analysis, design, simulation, validation, and testing. I also guided my student on the paper writing.

Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and **Nan Sun,** "A 10.5-b ENOB 645nW 100kS/s SAR ADC with Statistical Estimation Based Noise Reduction", *Custom Integrated Circuit Conference (CICC),* pp. 1-4, Sept. 2015.

- Co-authors: Long, Xiyuan, Arindam, and Yeonam are all my PhD students. Jie is a PhD student at George Washington University.
- Qualitative statement of contribution: I came up with the original idea. I advised my

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students on the circuit analysis, design, simulation, validation, and testing. I also guided my students on the paper writing.

Kareem Ragab and **Nan Sun**, "A 12b ENOB, 2.5MHz-BW, 4.8mW VCO-Based 0-1 MASH ADC with Direct Digital Background Nonlinearity Calibration", *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2015.

- Co-authors: Kareem is my PhD student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis, design, simulation, validation, and testing. I also guided my student on the paper writing.

Nicholas Wood and **Nan Sun**, "Predicting ADC - a new approach to ADC design," *IEEE Dallas Circuits and Systems Conference (DCAS)*, pp. 1-4, Oct. 2014.

- Co-authors: Nicholas is an undergraduate student at UT Austin.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Arindam Sanyal, Kareem Ragab, Long Chen, T.R. Viswanathan, Shouli Yan, and **Nan Sun**, "A hybrid SAR-VCO delta-sigma ADC with first-order noise shaping," *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, 2014.

- Co-authors: Arindam, Kareem, and Long are my PhD students. TR is research professor at UT Austin. Shouli is design manager at On Semiconductor, Ltd.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis, design, simulation, validation, and testing. I also guided my student on the paper writing.

Long Chen, Arindam Sanyal, Ji Ma, and **Nan Sun**, "A 24-uW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique," *European Solid-State Circuit Conference (ESSCIRC)*, pp. 219-222, 2014.

- Co-authors: Long and Arindam are my PhD students. Ji is my Master's student.
- Qualitative statement of contribution: My student Arindam came up with original circuit idea. I advised my student on the circuit analysis, design, simulation, validation, and testing. I also guided my student on the paper writing.

K. R. Raghunandan, **Nan Sun**, and T.R. Viswanathan, "Analog signal processing in deep submicron CMOS technologies using inverters," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 394-397, 2014.

- Co-authors: TR is research professor at ECE Dept., UT Austin. K. R. Raghunandan is TR's PhD student.
- Qualitative statement of contribution: I offered technical feedback and guided the student on the paper writing.

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Arindam Sanyal and **Nan Sun**, "A low frequency-dependence, energy-efficient switching technique for bottom-plate sampled SAR ADC," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 297-300, 2014.

- Co-authors: Arindam is my PhD student.
- Qualitative statement of contribution: The student came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Xiankun Jin and **Nan Sun**, "Low-cost high-quality constant offset injection for SEIR-based ADC built-in-self-test," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 285-288, June 2014.

- Co-authors: Xiankun is my Master's student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Peijun Wang and **Nan Sun**, "A random DEM technique with minimal element transition rate for high-speed DACs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1155-1158, June 2014.

- Co-authors: Peijun is my Master's student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Long Chen, Ji Ma, and **Nan Sun**, "Capacitor mismatch calibration for SAR ADCs based on comparator metastability detection," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2357-2360, June 2014.

- Co-authors: Long is my PhD student. Ji is my Master's student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Arindam Sanyal and **Nan Sun**, "An enhanced ISI shaping technique for multi-bit delta sigma DACs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2341-2344, June 2014.

- Co-authors: Arindam is my PhD student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Yeonam Yoon, Kyoungtae Lee, and **Nan Sun**, "A purely-VCO-based single-loop high-order continuous-time delta sigma ADC," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 926-929, June 2014.

- Co-authors: Yeonam is my PhD student. Kyoungtae is my Master's student.

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- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Manzur Rahman, Long Chen, and **Nan Sun**, "Algorithm and implementation of digital calibration of fast converging radix-3 SAR ADC," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1336-1339, June 2014.

- Co-authors: Manzur and Long are my PhD students.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Kyoungtae Lee, Yeonam Yoon, and **Nan Sun**, "A 1.8mW 2MHz-BW 66.5dB-SNDR delta-sigma ADC using VCO-based integrators with intrinsic CLA," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-4, Sept. 2013.

- Co-authors: Kyoungtae is my Master's student. Yeonam is my PhD student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Long Chen, Manzur Rahman, Sha Liu, and **Nan Sun**, "A fast radix-3 SAR analog-to-digital converter," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1148-1151, Sept. 2013.

- Co-authors: Long and Manzur are my PhD students. Sha is a No Thesis/No Report Master's student in ECE.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Arindam Sanyal and **Nan Sun**, "A very high energy-efficiency switching technique for SAR ADCs," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 229-232, Aug. 2013.

- Co-authors: Arindam is my PhD student.
- Qualitative statement of contribution: My student came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Rohit Yadav and **Nan Sun**, "A 1.2mW 67.5 dB SQDR VCO-based sigma delta ADC with non-linearity cancellation technique," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 570-573, Aug. 2013.

- Co-authors: Rohit is a No Thesis/No Report Master's student in ECE. Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my student on the paper writing.

10

Kyoungtae Lee, Yeonam Yoon, and **Nan Sun**, "A 10MHz-BW, 5.6mW, 70dB SNDR delta-sigma ADC using VCO-based integrators with intrinsic DEM," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2006 - 2009, May 2013.

- Co-authors: Kyoungtae is my Master's student. Yeonam is my PhD student.
- Qualitative statement of contribution: I came up with the original idea. I advised my students on the circuit analysis and design. I also guided my students on the paper writing.

Wenjuan Guo, Youngchun Kim, Arindam Sanyal, Ahmed Tewfik, and **Nan Sun**, "A single SAR ADC converting multi-channel sparse signals," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2235 - 2238, 2013.

- Co-authors: Wenjuan and Arindam are my PhD students. Ahmed is a Professor in the ECE Dept. at UT Austin. Youngchun is Ahmed's PhD student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

Travis Forbes, Wei-Gi Ho, **Nan Sun**, and Ranjit Gharpurey, "A frequency-folded ADC architecture with digital LO synthesis," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 149-152, 2013.

- Co-authors: Ranjit is a Professor at ECE Dept., UT Austin. Travis and Wei-Gi are Ranjit's PhD students.
- Qualitative statement of contribution: I offered technical feedback and guided students on the paper writing.

Nan Sun, Yong Liu, Ling Qin, Guangyu Xu, and Donhee Ham, "Solid-state and biological systems interface," *Proceedings of European Solid-State Circuit Conference (ESSCIRC)*, Sept. 2012, pp. 14-17.

- Co-authors: Donhee is my PhD advisor at Harvard. Yong and Ling are Donhee's PhD students. Guangyu is Donhee's post-doc.
- Qualitative statement of contribution: This is an invited review paper. I developed most of the techniques reviewed in this paper. I also contributed to the writing of this paper.

Nan Sun, Hae-Seung Lee, and Donhee Ham, "A 2.9-mW 11-B 20-MS/s pipelined ADC with dual-mode-based digital background calibration," *Proceedings of European Solid-State Circuit Conference (ESSCIRC)*, Sep. 2012, pp. 269-272.

- Co-authors: Hae-Seung is professor at MIT. Donhee is my PhD advisor at Harvard.
- Qualitative statement of contribution: I came up with the original idea. I finished the majority of the circuit analysis, design, and validation. I also completed the paper writing.

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Arindam Sanyal and **Nan Sun**, "A simple and efficient dithering method for vector quantizer based mismatch-shaped $\Delta\Sigma$ DACs," *IEEE Proceedings of International Symposium on Circuits and Systems*, pp. 528-531, 2011.

- Co-authors: Arindam is my PhD student.
- Qualitative statement of contribution: I came up with the original idea. I advised my student on the circuit analysis and design. I also guided my students on the paper writing.

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Nan Sun <sunnansunny@gmail.com>

IEEE Journal of Solid State Circuits - Decision on Manuscript ID JSSC-Apr-16-0189.R1

IEEE Journal of Solid State Circuits
<onbehalfof+chosta+ee.kaist.ac.kr@manuscriptcentral.com>
Reply-To: chosta@ee.kaist.ac.kr
To: kragab@utexas.edu
Cc: kragab@utexas.edu, nansun@mail.utexas.edu

Thu, Sep 22, 2016 at 3:35
AM

22-Sep-2016

Dear Mr. Ragab:

I am pleased to accept your submission, JSSC-Apr-16-0189.R1, "A 12b ENOB, 2.5MHz, 4.8mW VCO-Based 0-1 MASH with Direct Digital Background Calibration" for publication in the Journal of Solid State Circuits.

This acceptance is for the present form of your manuscript. No changes should be made with respect to the manuscript version.

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I look forward to reading your contribution in the IEEE Journal of Solid State Circuits.

Sincerely,
Prof. Seonghwan Cho
Associate Editor, IEEE Journal of Solid State Circuits
chosta@ee.kaist.ac.kr

Reviewer(s)' Comments to Author:

Reviewer: 1

Comments to the Author
The revised manuscript addressed most of the concerns raised in the previous review, and it can be accepted as is.

Reviewer: 2

Comments to the Author
Thank you for addressing my concerns.

Reviewer: 3

Comments to the Author
(There are no comments.)

[DR1]

J25

M Gmail

Nan Sun <sunnansunny@gmail.com>

IEEE Transactions on Circuits and Systems II: Express Briefs - Decision on Manuscript ID TCAS-II-00275-2016

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encktse@polyu.edu.hk <encktse@polyu.edu.hk>   Mon, Apr 18, 2016 at 8:27 AM
To: jackiechan.cl@utexas.edu
Cc: encktse@polyu.edu.hk, jackiechan.cl@utexas.edu, kragab@utexas.edu, felt26@utexas.edu,
arindam3110@utexas.edu, jeonggoo.song@utexas.edu, nansun@mail.utexas.edu

18-Apr-2016

Dear Dr. Chen:

It is our pleasure to accept your manuscript entitled "A 0.95-mW 6-b 700-MS/s Single-Channel Loop-Unrolled SAR ADC in 40-nm CMOS" for publication in the IEEE Transactions on Circuits and Systems II: Express Briefs, as an Express Letter. Final recommendations by the Associate Editor and Reviewers' Comments to improve your manuscript are included at the foot of this letter.

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Nan Sun <sunnansunny@gmail.com>

Message from Electronics Letters

eletters@theiet.org <eletters@theiet.org>   Tue, May 24, 2016 at 3:47 AM
To: arindam3110@utexas.edu, nansun@mail.utexas.edu, sunnansunny@gmail.com

Dear Dr. Arindam Sanyal

I am pleased to inform you that your paper ELL-2016-1428.R1 'A second-order VCO-based Delta Sigma ADC using a modified DPLL' has been accepted for publication in Electronics Letters and will appear in a forthcoming issue in the next few weeks. A complimentary version of the final published version of your paper will be sent to you in PDF format in due course.

To maintain the speed of publication, proofs are not sent to authors for checking before publication and author changes at this stage cannot normally be accepted.

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Fwd: ISCAS 2016 Decision Notification - Paper 1838

Long Chen <jackiechan.cl@utexas.edu>   Mon, Jan 11, 2016 at 1:28 PM
To: Arindam Sanyal <arindam3110@utexas.edu>, Ji Ma <martin.maji@gmail.com>, Xiyuan Tang <felt26@utexas.edu>, Nan Sun <nansun@mail.utexas.edu>

Dear Authors,

I am happy to let you know that the iscas paper has been accepted. Thanks for your support and help during the paper writing:)

Best,
Long
---------- Forwarded message ----------
From: <iscas@epapers.org>
Date: Mon, Jan 11, 2016 at 12:36 PM
Subject: ISCAS 2016 Decision Notification - Paper 1838
To: jackiechan.cl@utexas.edu
Cc: iscas@epapers.org

Dear Long Chen,

Congratulations !

Your paper number 1838 entitled "Comparator Common-Mode Variation Effects Analysis and its Application in SAR ADCs", has been accepted for Lecture presentation at the 2016 IEEE Int'l Symposium on Circuits & Systems, to be held in Montreal, Canada from May 22-26, 2016. We look forward to your participation and presentation at ISCAS 2016.

Your paper has been assigned to Data Converters III Lecture session C1L-E. The full Conference schedule will be available on the ISCAS 2016 web site very soon. Be sure to check the conference web site (http://iscas2016.org/) often as important information is posted regularly on this site. If there are additional co-authors for this paper, please make sure to inform them of this decision.

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Wenjuan Guo <wjguo@utexas.edu>   Tue, Jun 7, 2016 at 1:38 PM
To: Nan Sun <nansun@mail.utexas.edu>

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From: <ess@epapers.org>
Date: Tue, Jun 7, 2016 at 12:31 PM
Subject: ESSDERC/ESSCIRC 2016 Decision Notification - Paper 5049
To: wjguo@utexas.edu
Cc: ess@epapers.org

Dear Wenjuan Guo,

Congratulations !

Your paper number 5049 entitled "A 9.8b-ENOB 5.5fJ/Step Fully-Passive Compressive Sensing SAR ADC for
WSN Applications", has been accepted for Lecture presentation at ESSDERC/ESSCIRC 2016, to be held in
Lausanne, Switzerland from   12-15 September 2016. We look forward to your participation and presentation.

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M Gmail   **Nan Sun <sunnansunny@gmail.com>**

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Shaolan Li <slliandy@gmail.com>   Tue, Jun 7, 2016 at 1:08 PM
To: Nan <nansun@mail.utexas.edu>

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From: <ess@epapers.org>
Date: Jun 7, 2016 12:33 PM
Subject: ESSDERC/ESSCIRC 2016 Decision Notification - Paper 5099
To: <slliandy@utexas.edu>
Cc: <ess@epapers.org>

Dear Shaolan Li,

Congratulations !

Your paper number 5099 entitled "A 174.3dB FoM VCO-Based CT ?? Modulator with a Fully Digital Phase
Extended Quantizer and Tri-Level Resistor DAC in 130nm CMOS", has been accepted for Lecture presentation
at ESSDERC/ESSCIRC 2016, to be held in Lausanne, Switzerland from   12-15 September 2016. We look
forward to your participation and presentation.

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Nan Sun <sunnansunny@gmail.com>

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Kareem Ragab <kragab@utexas.edu>   Tue, Jun 7, 2016 at 12:59 PM
To: Nan Sun <nansun@mail.utexas.edu>

Dear Nan,

FYI, the official notification is out.

Best Regards,
Kareem
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From: <ess@epapers.org>
Date: Tue, Jun 7, 2016 at 10:37 AM
Subject: ESSDERC/ESSCIRC 2016 Decision Notification - Paper 5201
To: kragab@utexas.edu
Cc: ess@epapers.org

Dear Kareem Ragab,

Congratulations !

Your paper number 5201 entitled "A 1.4mW 8b 350MS/S Loop-Unrolled SAR ADC with Background Offset Calibration in 40nm CMOS", has been accepted for Lecture presentation at ESSDERC/ESSCIRC 2016, to be held in Lausanne, Switzerland from 12-15 September 2016. We look forward to your participation and presentation.

The technical program is still being finalized and the full conference schedule will be available on the ESSDERC/ESSCIRC 2016 web site very soon. Be sure to check the conference web site (http://esscirc-essderc2016.epfl.ch/) often as important information is posted regularly on this site. If there are additional co-authors for this paper, please make sure to inform them of this decision.

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Nan Sun <sunnansunny@gmail.com>

Fwd: ESSDERC/ESSCIRC 2016 Decision Notification - Paper 5113

Arindam Sanyal <arindam3110@utexas.edu>   Tue, Jun 7, 2016 at 1:08 PM
To: Nan <nansun@mail.utexas.edu>

Dear Nan,

We have the confirmation from ESSCIRC.

Thanks
Arindam

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> **From:** <ess@epapers.org>
> **Date:** June 7, 2016 at 12:34:06 PM CDT
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> **Cc:** <ess@epapers.org>
> **Subject: ESSDERC/ESSCIRC 2016 Decision Notification - Paper 5113**
> **Reply-To:** <ess@epapers.org>

Dear Arindam Sanyal,

Congratulations !

Your paper number 5113 entitled "A 55fJ/conv-Step Hybrid SAR-VCO Delta Sigma Capacitance-to-Digital Converter in 40nm CMOS", has been accepted for Lecture presentation at ESSDERC/ESSCIRC 2016, to be held in Lausanne, Switzerland from   12-15 September 2016. We look forward to your participation and presentation.

The technical program is still being finalized and the full conference schedule will be available on the ESSDERC/ESSCIRC 2016 web site very soon. Be sure to check the conference web site (http://esscirc-essderc2016.epfl.ch/) often as important information is posted regularly on this site. If there are additional co-authors for this paper, please make sure to inform them of this decision.

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Nan Sun <sunnansunny@gmail.com>

Fwd: ESSDERC/ESSCIRC 2016 Decision Notification - Paper 5265

Xiyuan Tang <felt26@utexas.edu>   Thu, Jun 9, 2016 at 9:29 AM
To: "nansun@mail.utexas.edu" <nansun@mail.utexas.edu>

Dear Nan,

Sorry that I forgot.

Thanks!
Xiyuan

---------- Forwarded message ----------
From: <ess@epapers.org>
Date: Tue, Jun 7, 2016 at 12:39 PM
Subject: ESSDERC/ESSCIRC 2016 Decision Notification - Paper 5265
To: felt26@utexas.edu
Cc: ess@epapers.org

Dear Xiyuan Tang,

Congratulations !

Your paper number 5265 entitled "A 10-B 750 W 200MS/S Fully Dynamic Single-Channel SAR ADC in 40nm
CMOS", has been accepted for Lecture presentation at ESSDERC/ESSCIRC 2016, to be held in Lausanne,
Switzerland from   12-15 September 2016. We look forward to your participation and presentation.

The technical program is still being finalized and the full conference schedule will be available on the
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UT Austin_0014325

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M Gmail   **Nan Sun <sunnansunny@gmail.com>**

Fwd: ESSDERC/ESSCIRC 2016 Decision Notification - Paper 5102

Wenjuan Guo <wjguo@utexas.edu>   Tue, Jun 7, 2016 at 1:38 PM
To: Nan Sun <nansun@mail.utexas.edu>

---------- Forwarded message ----------
From: <ess@epapers.org>
Date: Tue, Jun 7, 2016 at 12:33 PM
Subject: ESSDERC/ESSCIRC 2016 Decision Notification - Paper 5102
To: wjguo@utexas.edu
Cc: ess@epapers.org

Dear Wenjuan Guo,

Congratulations !

Your paper number 5102 entitled "A 12b-ENOB 61㙟 Noise-Shaping SAR ADC with a Passive Integrator", has been accepted for Lecture presentation at ESSDERC/ESSCIRC 2016, to be held in Lausanne, Switzerland from 12-15 September 2016. We look forward to your participation and presentation.

The technical program is still being finalized and the full conference schedule will be available on the ESSDERC/ESSCIRC 2016 web site very soon. Be sure to check the conference web site (http://esscirc-essderc2016.epfl.ch/) often as important information is posted regularly on this site. If there are additional co-authors for this paper, please make sure to inform them of this decision.

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4. Your author account username: Wenjuan
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C37

M Gmail   **Nan Sun <sunnansunny@gmail.com>**

Fwd: A-SSCC 2016 Decision Notification - Paper 4054

Jeonggoo Song <jeonggoo.song@utexas.edu>   Fri, Aug 5, 2016 at 12:16 PM
To: Nan <nansun@mail.utexas.edu>

Dear Professor,

Our paper got accepted! Thank you so much for all your help and support.

Thank you.

Sincerely,

Jeonggoo Song

---------- Forwarded message ----------
From: <asscc@epapers.org>
Date: Fri, Aug 5, 2016 at 10:39 AM
Subject: A-SSCC 2016 Decision Notification - Paper 4054
To: jeonggoo.song@utexas.edu
Cc: asscc@epapers.org

Dear Jeonggoo Song,

Congratulations !

Your paper number 4054 entitled "A 10-B 800MS/S Time-Interleaved SAR ADC with Fast Timing-Skew Calibration", has
been accepted for Lecture presentation at 2016 IEEE Asian Solid-State Circuits Conference, to be held in Toyama, Japan
from November 7-9, 2016. We look forward to your participation and presentation at A-SSCC 2016.

Your paper has been assigned to Session 6 - HIGH-SPEED ADCS. The full Conference schedule is available at
http://www.a-sscc2016.org/Program-.php. (You can find your presentation time here). Be sure to check the conference
web site (http://www.a-sscc2016.org/) often as important information is posted regularly on this site. If there are additional
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http://www.epapers.org/asscc2016. Your paper must comply with the specifications outlined on the web site. Due to
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4. Your author account username: songjeonggoo
5. Need your password? Click the "Forgot your Password?" link in the log-in box of the submission site
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Budget Council Assessment of
Dr. Nan Sun's Teaching Performance

This Budget Council assessment of Professor Sun's teaching is based on a thorough evaluation of the materials assembled by the candidate for promotion to associate professor, direct observation of the candidate's teaching, evaluation of course materials, and detailed examination of course instructor survey numerical ratings and student comments.

Principal Areas of Teaching

Professor Sun teaches courses in the important area of circuit design. In teaching, Professor Sun draws upon his research and prototyping experience in analog/mixed-signal integrated circuit design. Integrated circuit design concerns the design, simulation, fabrication and testing of circuits on a single chip. This miniaturization is critical to reduce the size, weight and power consumption of circuits for inclusion into a product. For example, the audio system of a smart phone consists of a converter from a digital audio stream to an analog audio signal for playback over speakers or headphones. The converter is a mixed-signal integrated circuit in that it processes a digital input signal to produce an analog output signal. In addition, the audio playback system also includes miniaturized amplifiers to control the playback volume.

Professor Sun has taught key undergraduate and graduate courses in analog and mixed-signal circuit design. His first course, in spring 2011, was EE 338K *Electronic Circuits II*. This course concerns general analytical and simulation principles useful for both board-level and integrated circuit design. He revamped the course, including modernizing lecture content, developing homework assignments and introducing a design project. Students responded really well, as mentioned in the next section. Other faculty continued to build on his overhaul of EE 338K.

Because analog/mixed-signal IC design is understaffed in terms of faculty, Professor Sun has been teaching the fundamental analog integrated circuit (IC) design course as a crosslisted undergraduate and graduate course, EE 338L/382M-14 *Analog IC Design*. This course includes the analysis and design of analog integrated circuits, and the use of integrated circuit tools and technology to design fundamental analog circuit blocks for a wide range of applications. For this course, he created new homework assignments and added a design project. The design project became part of a new in-class student design contest.

His third course is an advanced graduate course in mixed-signal integrated circuit design, EE 382V *Data Converters*. This course deals with the design of data converters, which convert digital signals to analog signals, or vice-versa. Data converters are critical for transmitting and receiving communication signals (Wi-Fi, cellular, Bluetooth, etc.) and recording and playing back speech/audio streams. There are many data converters in smart phones, sound systems, TVs, biomedical instruments, and many other products. He completely redesigned the course, including adding a student design contest.

Professor Sun represents a key, and understaffed, area at both the undergraduate and graduate levels in the department. In his courses, he covers topics that are in great demand by industry, including several companies in Austin. Moreover, a large number of

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graduate students are interested in working with him.

Teaching Evaluation Procedures and Measures

The department employs two methods to evaluate teaching performance: Course Instructor Surveys and Peer Observations of Classroom Instruction. The course instructor surveys are conducted in the last three weeks of lecture in every course. A peer evaluation is carried out by a senior faculty member after a visit to the classroom. The time and date of the visit are generally agreed on, in advance, between the instructor and the evaluator, and the evaluation is reviewed by both the instructor and evaluator following the classroom visit.

Summary of Courses Taught and Course Instructor Surveys

The table below shows the courses taught by Professor Sun, the enrollments and the Course Instructor Survey (CIS) overall instructor and course ratings. His teaching ratings are excellent and well above the average for the department and college. For example, the departmental averages for the overall instructor ratings were 4.1 in spring 2012, fall 2012, spring 2014, and fall 2014, and 4.2 in spring 2011, spring 2013, spring 2015, and fall 2015.

Semester	Course Number	Course Title	Enrollment	Instructor Rating	Course Rating
Spr. 11	EE 338K	Electronics Circuits II	41	4.8	4.5
Spr. 12	EE 382V	Data Converters	20	5.0	4.9
Fall 12	EE 338L	Analog Integrated Circuit Design	57	4.5	4.3
Spr. 13	EE 382V	Data Converters	15	4.9	4.8
Spr. 14	EE 382V	Data Converters	10	4.6	4.6
Fall 14	EE 338L	Analog Integrated Circuit Design	58	4.6	4.4
Spr. 15	EE 382V	Data Converters	10	4.8	4.3
Fall 15	EE 338L	Analog Integrated Circuit Design	58	4.3	4.0

In the above semesters, the course instructor surveys for EE 338L *Analog Integrated Circuit Design* included those from the cross-listed course, EE 382M-14 *Analog Integrated Circuit Design*. The enrollment in EE 338L/382M-14 has been about 50% undergraduates and 50% graduate students.

In Spring 2016, Professor Sun was on modified service.

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One way to evaluate Professor Nan Sun is to compare his teaching to the other professors who taught the same courses in recent years, as shown in the table below. In EE 338K, Professor Sun had a higher overall instructor rating when compared to the average overall instructor rating for the three faculty who taught EE 338K in recent years. This is also true for EE 382V. In EE 338L, Professor Sun's overall instructor rating is between the first and second average overall instructor ratings of his colleagues given below.

Instructor	Course Number	Course Title	Instructor Rating	Course Rating
Professor #1	EE 338K	Electronics Circuits II	3.90	3.80
Professor #2	EE 338K	Electronics Circuits II	4.15	3.95
Professor #3	EE 338K	Electronics Circuits II	4.71	4.46
Professor #4	EE 338L	Analog IC Design	3.90	3.58
Professor #5	EE 338L	Analog IC Design	4.22	4.03
Professor #6	EE 338L	Analog IC Design	4.60	4.30
Professor #7	EE 382V	Data Converters	3.20	3.20
Professor #8	EE 382V	Data Converters	4.28	4.06

Summary of Peer Observation of Classroom Instruction

Five peer evaluations were conducted for Professor Sun.
- Professor Hao Ling, Spring 2012
- Professor Edward Yu, Spring 2013
- Professor Jacob Abraham, Spring 2014
- Professor Seth Bank, Spring 2015
- Professor John Pearce, Spring 2016 (he evaluated a guest lecture by Professor Sun in the core undergraduate class, EE 313, *Linear Systems and Signals* (since Professor Sun was on family leave that semester, and did not teach a regular class).

The evaluations are uniformly glowing, as can be seen from the statements made by the evaluators.
EE 313, Linear Systems and Signals
- "Dr. Sun is an extraordinarily effective teacher"
- "He has obvious enthusiasm for the material ..."
- "His chosen delivery material is hand written notes in real time on the document camera. This is an effective method ..."
- "...I overheard students complimenting Dr. Sun's teaching style."

EE 383V, Data converters
- "Enthusiastic. Clearly enjoys what he is teaching"
- "...lecture style is dynamic and conversational ..."
- "The lecture slides are very detailed, thorough, and well constructed."
- "In more analytical discussions, Prof. Sun did a very nice job of explaining ... going to the whiteboard to supplement the material on the slides"

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- Always solicited questions. Students asked many questions and stayed engaged throughout the lecture."
- "Knowledgeable, and brought state-of-the-art research ideas into his lecture"

Individual Instruction

Professor Sun has graduated four PhD students while he was an Assistant Professor, three under his sole supervision, and one student who was co-supervised. One of his students is a tenure-track faculty member at SUNY Buffalo, and the others joined industry. He has also supervised 14 M.S. theses or reports. He is supervising 9 PhD students as sole supervisor and 2 who are co-supervised. This load is well above the average for a faculty member in the ECE department.

Summary

Professor Nan Sun is one of the top instructors in the ECE Department who has taught key courses in the field of Integrated Circuits at both the undergraduate and graduate levels. His courses provide our students with expertise that is in great demand by companies in Analog Design, including several in Austin. His CIS instructor ratings are outstanding and in the top tier of CIS instructor ratings in the department. He has been very successful in graduate student supervision, with three students receiving Ph.D.s under his sole supervision and one additional co-advised Ph.D. He has also graduated 14 M.S. students. He currently supervises a large and active group of M.S. and Ph.D. students (he has 9 Ph.D. students under his sole supervision). Professor Sun's performance in teaching clearly exceeds the standard for promotion to Associate Professor with tenure.

Submitted on behalf of the ECE Budget Council by

Jacob A. Abraham

Jacob A. Abraham
August 11, 2016

Brian L. Evans

Brian L. Evans
August 11, 2016

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Teaching Statement

Nan Sun
Department of Electrical and Computer Engineering
The University of Texas at Austin
nansun@mail.utexas.edu

I love teaching, and that's why I choose to be a professor. I aspire to be a teacher who continues to deepen my own field of science and maximally share my excitement about science with students in ways that help them learn fundamental ideas by heart, develop analytical skills, intuition, and the ability to see the big picture and apply what they learn to real-world applications. In addition to providing students with the knowledge and skills they need for their professional careers, I want to inspire them with the beauty of science, triumphs of engineering, and courageous journey of human minds. Ultimately, through my teaching, I want to help students develop positive outlooks that contribute to improvements in our lives.

1. Summary of Teaching Activities

I teach four different courses at UT-Austin:

EE 338K, *Electronic Circuits II,* is a junior- and senior-level course taken by ECE undergraduate students who choose the technical core of electronics and integrated circuits (IC). It covers the analysis and design of analog electronic circuits, including operational amplifier based circuits, power amplifiers, passive and active analog filters, as well as relaxation oscillators. I taught this course in Fall 2011. Its enrollment is between 40~50 students each year.

EE 338L, *Analog Integrated Circuit Design* is a senior-level course taken by undergraduates in ECE. This course covers the analysis and design of analog integrated circuits, such as operational amplifiers (op-amp), current mirrors, analog filters, etc. This class has a major final design project. Students use state-of-the-art computer aided design (CAD) tools to design a high-performance op-amp while meeting a list of design specifications. Its enrollment is between 30~40 undergraduate students each year.

EE 382M-14, *Analog Integrated Circuit Design* is a graduate-level course cross-listed with EE 338L. It is the first analog IC design class that graduate students take. This class meets together with the undergraduate students in EE 338L. The difference between EE 338L and EE 382M-14 is that graduate students are asked to solve more difficult homework and exam problems. The performance requirements on the final project are also higher. Its enrollment is between 30~40 graduate students each year.

EE 382V, *Data Converters* is a graduate-level course. The course teaches the analysis and design of analog-to-digital and digital-to-analog converters. It includes both architectural-level and transistor-level design considerations, sample-and-hold circuits, voltage comparators, noise analysis for mixed-signal circuits, and design trade-offs among power, noise, linearity, and speed. This course is offered every spring semester, with an enrollment of 10~20 graduate students each year.

1

CIS results for all courses that I taught are summarized in Table I.

TABLE I. CIS Results

Course	Semester	Enrollment / Returned	Instructor / Course Rating
EE 438K: *Analog Electronics*	Spring 11	41 / 24	4.8 / 4.5
EE 338L/382M-14: *Analog Integrated Circuit Design*	Fall 12	55 / 37	4.5 / 4.3
	Fall 14	52 / 39	4.6 / 4.4
	Fall 15	53 / 33	4.3 / 4.0
EE 382V: *Data Converters*	Spring 12	20 / 19	5.0 / 4.9
	Spring 13	15 / 14	4.9 / 4.8
	Spring 14	10 / 10	4.6 / 4.6
	Spring 15	10 / 9	4.8 / 4.3

In addition to classroom instruction, I have mentored five senior design teams, totaling ten semesters of supervision from 2011 to 2016. One project on a soil sensing system won *2nd place* at the end-of-year senior design competition. Another project on a low-power handheld bird call recorder won *top 10 nationwide* in Texas Instruments (TI) Analog Design Competition in 2013. The entire team and I were invited to TI headquarters in Dallas for the award ceremony.

I have also been very active in organizing technical seminars for both undergraduate and graduate students. Over the past 5 years, I have organized more than 50 talks given by both academic and industry experts. These talks substantially benefit students and are great additions to the regular classroom teaching.

2. Teaching Philosophy and Methodologies

In terms of teaching methodologies, I focus on intuition very heavily. Whenever I teach a difficult subject, I always try to use a few simple sentences to explain the intuition first. I like to make analogies so that the fundamental reasoning behind the difficult concept is easy to grasp. Mathematics is very important, and it is the language that we use to accurately describe a theory. Nevertheless, if concepts are presented mainly in the format of mathematical derivations, students find them hard to follow and uninteresting. Moreover, this is not the way that innovations are made. Researchers are always guided by their intuitions. Mathematics is a tool that we use to formally establish a theory after we have already roughly formulated it using our intuitive reasoning. Through my teaching, I want to help students develop their own intuition and internalize it, and not just understand what is taught in the class, because I have always found intuition to be the most important element in my own academic endeavor.

I solidly believe that any engineering class should closely link theory with practice. The classes that I teach at UT are on integrated circuit (IC) design. While I cover many analytical methods, I believe that students learn best by applying these methods in a real-world engineering design project. For all the classes that I teach, I have a major design project with real-world performance specifications. I want to turn a student from a homework/exam problem solver into a real-world

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designer. Solving a homework problem is easy. There is only one answer, as the problem has already been well defined. Design is much more complicated and fundamentally different. There is no clear route. Nothing is fixed except for a final requirement. It involves frequent decision making and multi-dimensional optimization. Students who are good at homework and exams may not be good at design. The best way to teach design skills is to have a solid design project. Thus, I have paid special attention to developing a good design project. I prepare detailed handouts to guide them and reduce the slope of their learning curve, considering that their time is limited, but I do give them challenging design specifications so that they have to work hard and practice all the analytical techniques covered in the class. Students find the project very helpful. Many of them have told me that they truly understand theories only after they have used them in their project.

Since IC design is closely related to industry practices, setting up close interactions with industry greatly benefits the students' learning experience. Austin has many IC design companies. I have made a significant effort to establish a close relationship with local industry. I have successfully raised funding from industry and turned the class project into an industry sponsored *student design contest* with a monetary award. Industry experts are invited to serve as mentors and provide feedback on students' design projects. They helped formulate the project topic and served as judges for students' final presentations. I observed many positive outcomes of involving companies (e.g., Texas Instruments) in the class. First, since students recognized the importance of the project to real-world applications, they showed much stronger interest and worked much harder on the project (partly due to the prize money). Second, by communicating with industry engineers and receiving their feedback, students understand practical design considerations (such as area, yield, and reliability) much more deeply and are better prepared for careers in industry. So far, I have organized 6 student design contests. Organizing them takes a lot of extra energy, but I find it worthwhile. Students are motivated, and they learn much more.

I also believe that students learn most effectively when learning is fun and interactive. I like to make learning interesting and engaging. I frequently ask multi-choice questions during the class, and after pausing for a minute or so, I ask them to raise their hands to show me their choices. Students learn more when they are asked to first think by themselves about how to solve a problem. Before presenting my solutions, I ask students to explain theirs. Through these questions, I can engage the entire class and draw their attention. Students that choose wrong answers are motivated to follow my explanations and learn new materials.

As a professor, I like to have close interactions with my students and show that I care about them. I come to the classroom early so that I can chat with students who want to ask questions before class. After the class, I stay in the classroom to answer questions and leave only after all students have left. Students are encouraged to ask questions outside my office hours as well, and I try to make myself available to them as much as I can. I always reply to students' questions as soon as I can, as I believe that a quick reply shows that I have made their request a top priority.

I always like to explore the use of state-of-the-art technologies for innovative teaching. I have been using the Piazza software for the past two years. It is an online forum where students can post questions, and it is an efficient Q&A platform. For example, last semester, there were in

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total 241 questions posted. The TAs and I posted 243 responses. The most amazing thing is that for these 241 questions, *we have achieved a short average response time of only 30 minutes.* I believe that these fast interactions between students and instructors can greatly spur the enthusiasm of students towards learning. When students feel that professors care about them, trust is formed, and this is a key to a successful class.

3. Course Development

I have developed new lecture notes, homework problems, and exams for all four courses that I teach, and I update them every semester. I always want to bring the latest technical developments into the classroom so that students can be exposed to fresh ideas. I use textbooks, but never blindly follow them. I develop my own lecture notes and use them to explain the key concepts in a way that I feel are the most intuitive and accurate. Sometimes, I intentionally point out limitations and errors in a textbook so that students learn how important it is to develop one's own deep understanding. It is never a good idea to blindly follow any authority. Developing new notes takes a lot of time, but it makes teaching much more effective. Students like to know how a professor solves a problem in his/her own way, instead of simply repeating textbooks. Because I can always find better ways to explain the course materials, many students have encouraged me to write my own textbook. I have already collected a lot of materials for the new textbook, and I plan to finish it in three years.

4. Teaching Recognitions

In 2016, I was nominated by the ECE department for the Cockrell School of Engineering's Award for Outstanding Engineering Teaching by an Assistant Professor. In 2013, I was recognized for outstanding teaching from IEEE HKN UT Austin student chapter and selected by the graduating senior class as the professor who is most likely to write a book if he/she has not written one.

5. Individual Instructions

Student	Degree	Status	Start Date	Completion
Arindam Sanyal[1]	Ph.D.	Graduated	Fall 2011	Spring 2016
Wenjuan Guo[2]	Ph.D.	Graduated	Fall 2011	Spring 2016
Long Chen[3]	Ph.D.	Graduated	Fall 2011	Spring 2016
Kareem Ragab[4]	Ph.D.	Graduated	Fall 2011	Summer 2016
Yeonam Yoon	Ph.D.	In Candidacy	Fall 2011	Spring 2017 (est.)
Raghunadan Raghunathan	Ph.D.	In Candidacy	Fall 2011	Spring 2017 (est.)
Manzur Rahman	Ph.D.	In Candidacy	Fall 2012	Spring 2017 (est.)
Mikel Ash	Ph.D.	Pre-candidacy	Fall 2012	Fall 2017 (est.)
Shaolan Li	Ph.D.	Pre-candidacy	Fall 2012	Fall 2017 (est.)
Songjin Hong	Ph.D.	Pre-candidacy	Fall 2012	Fall 2017 (est.)
Miguel Gandara	Ph.D.	Pre-candidacy	Fall 2012	Fall 2017 (est.)
Xiyuan Tang	Ph.D.	Pre-candidacy	Fall 2012	Spring 2018 (est.)
Jeonggoo Song	Ph.D.	Pre-candidacy	Fall 2013	Spring 2018 (est.)
Linxiao Shen	Ph.D.	Pre-candidacy	Fall 2014	Spring 2019 (est.)
Abhishek Mukerjee	Ph.D.	Pre-candidacy	Fall 2014	Spring 2019 (est.)
Harold Bautista	M.S.	Graduated	Fall 2009	Spring 2012

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Marco Moreno	M.S.	Graduated	Fall 2010	Spring 2012
Miguel Gandara	M.S.	Graduated	Fall 2010	Spring 2012
Alex Fontaine	M.S.	Graduated	Fall 2011	Spring 2013
Shitong Zhao	M.S.	Graduated	Fall 2011	Spring 2013
Xiankun Jin	M.S.	Graduated	Fall 2011	Spring 2013
Olga Kardonik	M.S.	Graduated	Fall 2011	Spring 2013
Kyoungtae Lee	M.S.	Graduated	Fall 2012	Spring 2014
Ji Ma	M.S.	Graduated	Fall 2012	Spring 2014
You Li	M.S.	Graduated	Fall 2013	Spring 2015
Anoosh Gnana	M.S.	Graduated	Fall 2013	Spring 2015
Phillippe Dollo	M.S.	Graduated	Fall 2014	Spring 2016
Paridhi Gulati	M.S.	Graduated	Fall 2014	Spring 2016
Sowmya Katragadda	M.S.	Graduated	Fall 2014	Spring 2016
Jiawen Fu	M.S.	1st-year	Fall 2015	Spring 2017 (est.)
Chang Liu	M.S.	1st-year	Fall 2015	Spring 2017 (est.)

[1] Arindam Sanyal is a tenure-track assistant professor at State University of New York at Buffalo.

[2] Wenjuan Guo is with Intel, a top IC company.

[3] Long Chen is with Broadcom Ltd, also a top IC company.

[4] Kareem Ragab is with Broadcom Ltd.

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Appendix: Additional Tables

Table A1. Teaching Summary

Metric	Value
Number of Students Taught	256
Average Instructor Evaluation for UG Courses	4.55
Average Instructor Evaluation for Grad Courses	4.83
Average Course Evaluation UG Courses	4.30
Average Course Evaluation Grad Courses	4.65

Table A2. Course schedule by semester in EE since 2011; number of students indicated.

Course	S 11	F 11[1]	S 12	F 12	S 13	F 13[2]	S 14	F 14	S 15	F 15	S 16[3]
EE 338K	41	--	--	--	--	--	--	--	--	--	--
EE 338L/382M	--	--		55	--	--	--	52	--	53	--
EE 382V	--	--	20	--	15	--	10	--	10		--

[1] ECE dept. allows new assistant professor to teach 1 course in the first year, so I did not teach in F 11.
[2] I had a reduced teaching load as my first child was born in F 13.
[3] I had a reduced teaching load as my second child was born in S 16.

Table A3. Summary of Current Graduate Students Supervised at UT-Austin

Student	Co-Supervisor	Degree	Start Date	Date Reached Candidacy	Date Expected to Reach Candidacy	Expected Graduation Date
Raghunadan Raghunathan	TR Viswanathan	PhD	09/2010	04/2013	--	Spring 2017
Manzur Rahman	--	PhD	09/2012	02/2015	--	Spring 2017
Yeonam Yoon	--	PhD	09/2011	12/2015	--	Spring 2017
Mikel Ash	--	PhD	09/2012	--	Fall 2016	Fall 2017
Shaolan Li	--	PhD	09/2012	--	Fall 2016	Fall 2017
Songjin Hong	--	PhD	09/2012	--	Fall 2016	Fall 2017
Miguel Gandara	--	PhD	09/2012	--	Fall 2016	Fall 2017
Xiyuan Tang	--	PhD	09/2013	--	Spring 2017	Spring 2018
Jeonggoo Song	--	PhD	09/2013	--	Spring 2017	Spring 2018
Linxiao Shen	Nanshu Lu	PhD	09/2014	--	Fall 2017	Spring 2019
Abhishek Mukerjee	--	PhD	09/2014	--	Fall 2017	Spring 2019
Jiawen Fu	--	MS	09/2015	--	--	Spring 2017
Chang Liu	--	MS	09/2015	--	--	Spring 2017

6

Nan Sun
Department of Electrical and Computer Engineering
Course Rating Averages

What source was used to complete this chart? My CIS

EE 338K: Electronic Circuit II

Semester	Class Size	Number of Responses	Instructor Rating	Course Rating
Spring 11	41	24	4.8	4.5
Mean	**41**	**24**	**4.8**	**4.5**

EE 338L: Analog IC Design

Semester	Class Size	Number of Responses	Instructor Rating	Course Rating
Fall 12	57	37	4.5	4.3
Fall 14	58	39	4.6	4.4
Fall 15	58	33	4.3	4.0
Mean	**58**	**36**	**4.5**	**4.2**

EE 382V: Data Converters

Semester	Class Size	Number of Responses	Instructor Rating	Course Rating
Spring 12	20	19	5	4.9
Spring 13	15	14	4.9	4.8
Spring 14	11	10	4.6	4.6
Spring 15	10	10	4.8	4.3
Mean	**14**	**13**	**4.8**	**4.7**

SUN, NAN

09/01/16

Engineering
Electrical Engineering

Summary of Recent (All Years In Rank) UT Austin Course-Instructor Survey Resul
Overall Course/Instructor Items

| Semester	Course Number	Course Title	Enrollment		Instructor Averages*		College/School Averages**		
			No. of Students Enrolled on 12th Class Day	No. of Surveys Returned at End of Semester	Overall Instructor Rating	Overall Course Rating	Overall Instructor Rating	Overall Course Rating	No. Classes Surveyed
					Avg.	Avg.	Avg.	Avg.	
Spring 11	E E 338K	ELECTRONIC CIRCUITS II	41	24	4.8	4.5	N/A ***	N/A ***	N/A
Fall 11	E E 397M	GRADUATE RESEARCH INTERNSHIP	1	1	5.0	5.0	N/A ***	N/A ***	N/A
Spring 12	E E 382V	DATA CONVERTERS	20	19	5.0	4.9	N/A ***	N/A ***	N/A
Fall 12	E E 338L	ANALOG INTEGRATED CIRCUIT DSGN	57	37	4.5	4.3	N/A ***	N/A ***	N/A
Spring 13	E E 382V	DATA CONVERTERS	15	14	4.9	4.8	N/A ***	N/A ***	N/A
Spring 14	E E 382V	DATA CONVERTERS	11	10	4.6	4.6	N/A ***	N/A ***	N/A
Fall 14	E E 338L	ANALOG INTEGRATED CIRCUIT DSGN	58	39	4.6	4.4	N/A ***	N/A ***	N/A
Spring 15	E E 382V	DATA CONVERTERS	10	9	4.8	4.3	N/A ***	N/A ***	N/A
Fall 15	E E 338L	ANALOG INTEGRATED CIRCUIT DSGN	58	33	4.3	4.0	N/A ***	N/A ***	N/A

*For the computation of the averages, points were assigned to student responses as follows:
Excellent = 5, Very Good = 4, Satisfactory = 3, Unsatisfactory = 2, Very Unsatisfactory = 1

**College/school averages are the average of class averages, based on all courses surveyed in the instructor's college or school
during the academic year in which the course was taught.

***New CIS forms were implemented in the fall 2000 semester. The average rating on the overall course and instructor questions
on the new Basic and Expanded forms have been found to be approximately 0.1 to 0.2 points lower than those ratings on the old
Common form.

Prepared by the Measurement and Evaluation Center

Page 1
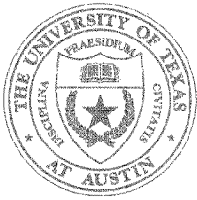
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
Cockrell School of Engineering

1616 Guadalupe St. • UTA Building, 7th Floor • Austin, Texas 78701
http://www.ece.utexas.edu/

2015-2016 Teaching Evaluation

Nan Sun, PhD; Assistant Professor
Department of Electrical and Computer Engineering

Prepared by: John A. Pearce
Temple Foundation Professor (#3)
May 5, 2016

I visited Prof. Zheng Wang's class, EE 313 *Linear Systems and Signals*, on May 4, 2016 to evaluate Nan Sun's teaching effectiveness as a guest lecturer that day. This was necessary because Dr. Sun has been on family leave this semester and is not currently teaching a scheduled EE class. The topic of the class was "Bodé Plots", a critically important topic for BSEE students due to its pervasive usefulness in all of electronics and signal analysis. As an overall summary, Dr. Sun is an extraordinarily effective teacher in my opinion, and the students received an excellent presentation of this important engineering tool. In fact, I learned a few techniques about the topic that I plan to use in my class next time it is taught. This evaluation has been shared with Dr. Sun this day.

Dr. Sun began the class by establishing rapport with the students. He did this easily. He has an obvious sense of humor that he uses to set an overall picture of the topic and its importance. Dr. Sun takes command of a class on time, and it is obvious that he plans to present some detailed material that he considers important. He has an adequate lecture volume and he has is no need of a microphone in this size room, ECJ 1.204. He speaks clearly and enunciates adequately. He has a very practical approach that makes it easy for the students to understand and put the material to use. He has obvious enthusiasm for the material that he maintains throughout the class period. He makes excellent use of class time and moves judiciously and moderately-paced through the topic without hurrying too much. The technical content is logical and complete.

His chosen delivery method is hand written notes in real time on the document camera. This is an effective method in my opinion because the students can see the concepts develop as they are presented in a step-by-step, logical, top-down fashion from basics to thorough in-depth analysis. The act of writing the development down in their notes forces them to interact with the material and summarize it.   This has been shown to be a more effective learning instrument than passive observation of a development for which the notes are completed ahead of time. As we were leaving the classroom I overheard students complimenting Dr. Sun's teaching style.

John Pearce

Classroom Review of **Nan Sun** by **Seth Bank**

On 3/4/2015, I met with Dr. Sun in advance of his lecture to discuss format and style, then attended his EE 382V: Data Converters lecture. The topic was generally voltage comparators, but the specific lecture was focused on multistage amplifiers and the relevant tradeoffs (time delay, voltage offset, etc.).

This course is a graduate course. 10 students were registered, but 16 students were in attendance, which includes auditors from UT and local industry. In my opinion, Dr. Sun is an excellent lecturer, with a natural conversational style and high bandwidth. His enjoyment and mastery of the subject were clear from both his delivery and in how he answered questions. I found his blend of intuitive explanations and mathematical rigor to be quite enjoyable and easy to follow.

Consistent with a graduate course, he maintained a rapid (though appropriate) pace during lecture, while still encouraging questions and back-and-forth with the students. His lecture notes were constructed in Powerpoint; the notes are clean, easy to read, and the text, equations, diagrams, and plots all speak to the topic at hand. It is clear that he has drawn and plotted virtually everything himself, which makes the lecture materials very quite easy to follow as they speak directly to the point he is making (e.g. there are no extraneous traces or diagrams that detract from the message). He is to be applauded for such high quality notes.

I discussed my feedback with Nan on 3/4/2015.

Sincerely,

Prof. Seth R. Bank
Temple Foundation Faculty Fellowship No. 5
Associate Professor

Peer Observation for Formative Assessment of Teaching

Faculty Member Observed _Nan Sun_____ Rank _Assistant Professor_

Date of Observation _April 2, 2014_____ Course Observed _EE 382V, Data Converters_____

	Not Applicable	Needs Improvement	Done Well	Truly Exemplary
CONTENT				
1. Presented main ideas clearly	NA	NI	DW	**TE**
2. Provided variety of supporting information	NA	NI	**DW**	TE
3. Clearly addressed relevancy of main ideas	NA	NI	DW	**TE**
4. Required higher order thinking of students	NA	NI	**DW**	TE
5. Related ideas to students' prior knowledge	NA	NI	DW	**TE**
6. Provided definitions for new terms/concepts	NA	NI	DW	**TE**
ORGANIZATION				
7. Connected introduction to previous classes	NA	NI	**DW**	TE
8. Stated organization/objectives	NA	NI	DW	**TE**
9. Used clear, effective transitions with summaries	NA	NI	DW	**TE**
10. Had a clear and organized plan	NA	NI	DW	**TE**
11. Concluded by summarizing main ideas	NA	NI	DW	**TE**
12. Connected to future classes/courses/expectations	NA	NI	**DW**	TE
INTERACTION				
13. Questioned students at different learning levels	NA	NI	**DW**	TE
14. Provided sufficient wait time after asking questions	NA	NI	**DW**	TE
15. Encouraged student questions	NA	NI	**DW**	TE
16. Gave informative responses to student questions	NA	NI	DW	**TE**
17. Had a good rapport/engagement with students	NA	NI	DW	**TE**
VERBAL/NONVERBAL				
18. Was confident and enthusiastic	NA	NI	DW	**TE**
19. Used clear articulation and pronunciation	NA	NI	**DW**	TE
20. Spoke extemporaneously	NA	NI	DW	**TE**
21. Minimized any distracting accent/language	NA	NI	**DW**	TE
22. Projected voice to be easily heard	NA	NI	**DW**	TE
23. Used appropriate pace of delivery	NA	NI	**DW**	TE
24. Made adequate eye contact with students	NA	NI	DW	**TE**
USE OF MEDIA				
25. Used classroom technology proficiently	NA	NI	**DW**	TE
26. Made visual aids easy to read	NA	NI	**DW**	TE
27. Provided effective outline/handouts	NA	NI	**DW**	TE

OVERALL RATING

	Unsatisfactory	Satisfactory	Very Good	Excellent
Overall, this instructor was				_Excellent_

Modified 1/2011/PJD

NARRATIVE RESPONSES

STRENGTHS [e.g. apparent knowledge of curriculum preceding and following the presented material, positive feedback to students, opportunity provided for student questions, pharmacy-relevant examples]:

Very good instructor, see ratings above

AREAS FOR IMPROVEMENT [e.g. inability to answer student questions, deficiencies in content knowledge, absence of examples/irrelevant examples, difficulties with student rapport, etc.]:

The only negative I saw was that he did not repeat student questions, so that if the question was asked from the front, the students in the back may not have heard it. The answers were consistently very clear. I made the suggestion to him that he should repeat questions from students, and believe that he will do that from now on.

ADDITIONAL COMMENTS BEYOND THE LECTURE [e.g. correlation between exam questions and learning objectives, reflection on and incorporation of previous review and suggestions for improvement in teaching, etc.]:

None.

OVERALL: An excellent instructor, and an asset to the department.

Date of Conference _April 2, 2014

Observer Signature   *Jacob A. Abraham*

Faculty Peer Teaching Evaluation   The University of Texas at Austin

Course: EE 382V   **Instructor:** Nan Sun   **Semester:** S13
Evaluator: Edward Yu   **Date of Evaluation:** 04/30/2013

Method of Evaluation:

Examination of course syllabus and online lecture notes, and in-person evaluation of class session on Tu 04/30/2013.

Prof Sun had the opportunity to review this evaluation prior to submission and provide comments and/or corrections (none were provided).

Clarity and Pace of Communication:
Includes quality of oral communication, boardwork and/or A/V presentation, etc.

The lecture started promptly at 5:00PM with a motivation for fabrication, measurement and testing of chips. Prof Sun's lecture style is very dynamic and conversational, with very good voice projection and eye contact, and the slides are effective in supporting the points he is making in the lecture without becoming too detailed or verbose.

Building upon the slides, Prof Sun provided a very nice discussion of complexities associated with high-performance chip testing, e.g., frequency range of signal source, distortion, etc. and very nicely connected practical specifications of actual sources with the impact of their performance limitations on data converter testing. He also did a good job in asking students how they might approach problems he posed to the class, for example in a discussion of filtering as a way to reduce distortion.

In more analytical discussions, e.g., of estimating jitter in clock signals, Prof Sun did a very nice job of explaining, fairly intuitively, a method for measuring jitter, going to the whiteboard to supplement the material on the slides.

Lecture ended with a recap of the key take-away message from the lecture.

Engagement with Students:
Includes general quality and nature of interaction, openness and responsiveness to questions, gauging student understanding and attentiveness, etc.

Students in the class were clearly attentive during the lecture. The large amount of specific, practical knowledge seemed to keep them engaged throughout, although there were somewhat fewer questions than might have been expected. It might be helpful to ask the class more frequently if they have questions.

Several students went up to Prof Sun with questions after the lecture, and he was clearly very open to discussion with students regarding the course material and project.

Quality of Course Material:
Includes (as appropriate) lecture content and context, supplementary materials, homework, exams, etc.

EE 382V provides a very thorough introduction to and discussion of data conversion generally, specific approaches for design of data converters, and performance metrics and applications. The lecture slides

are very detailed, thorough, and well constructed. They should be a valuable resource for students well after they have completed the course.

I did not have the opportunity to evaluate the homework assignments, project, and exams in detail, but from discussion with a student in the class it appears that the project is quite substantial.

Overall Comments:

Prof Sun is very skilled lecturer with a dynamic and engaging lecture style, and made very good use of a well constructed slide deck in his lecture. The lecture I observed contained a lot of very practical knowledge and insights, reflecting his knowledge and experience in this field, which were combined with more analytical discussions when appropriate. One suggestion would be to pause more frequently during the lectures to ask if the class has questions, or perhaps to ask questions of the class a bit more frequently to gauge understanding and elicit active responses.

Edward T. Yu, Professor of Electrical & Computer Engineering

Peer Observation for Formative Assessment of Teaching

Faculty Member Observed __Nan Sun__   Rank __Assistant Professor__

Date of Observation __4/4/12__   Course Observed __EE383V (Data Converters)__

	Not Applicable	Needs Improvement	Done Well	Truly Exemplary
CONTENT				
1. Presented main ideas clearly	NA	NI	(DW)	TE
2. Provided variety of supporting information	NA	NI	(DW)	TE
3. Clearly addressed relevancy of main ideas	NA	NI	(DW)	TE
4. Required higher order thinking of students	NA	NI	(DW)	TE
5. Related ideas to students' prior knowledge	NA	NI	(DW)	TE
6. Provided definitions for new terms/concepts	NA	NI	(DW)	TE
ORGANIZATION				
7. Connected introduction to previous classes	NA	NI	(DW)	TE
8. Stated organization/objectives	NA	(NI)	DW	TE
9. Used clear, effective transitions with summaries	NA	NI	(DW)	TE
10. Had a clear and organized plan	NA	NI	(DW)	TE
11. Concluded by summarizing main ideas	NA	NI	(DW)	TE
12. Connected to future classes/courses/expectations	NA	NI	(DW)	TE
INTERACTION				
13. Questioned students at different learning levels	NA	NI	(DW)	TE
14. Provided sufficient wait time after asking questions	NA	NI	(DW)	TE
15. Encouraged student questions	NA	NI	DW	(TE)
16. Gave informative responses to student questions	NA	NI	DW	(TE)
17. Had a good rapport/engagement with students	NA	NI	DW	(TE)
VERBAL/NONVERBAL				
18. Was confident and enthusiastic	NA	NI	DW	(TE)
19. Used clear articulation and pronunciation	NA	NI	(DW)	TE
20. Avoided verbalized pauses (e.g. er, ah, um, etc.)	NA	NI	(DW)	TE
21. Spoke extemporaneously	NA	NI	(DW)	TE
22. Minimized any distracting accent/language	NA	(NI)	DW	TE
23. Projected voice to be easily heard	NA	NI	(DW)	TE
24. Used appropriate pace of delivery	NA	NI	(DW)	TE
25. Made adequate eye contact with students	NA	NI	DW	(TE)
USE OF MEDIA				
26. Used classroom technology proficiently	NA	NI	(DW)	TE
27. Made visual aids easy to read	NA	(NI)	DW	TE
28. Provided effective outline/handouts	NA	NI	(DW)	TE

OVERALL RATING

Overall, this instructor was   *Unsatisfactory*   *Satisfactory*   *Very Good*   (*Excellent*)

Modified 1/2011/PJD

NARRATIVE RESPONSES

STRENGTHS [e.g. apparent knowledge of curriculum preceding and following the presented material, positive feedback to students, opportunity provided for student questions, pharmacy-relevant examples]:

- Enthusiastic. Clearly enjoys what he is teaching.
- Good hand gesture. Good eye contact.
- Always solicited questions. Students asked many questions and stayed engaged throughout the lecture. Was very honest when he did not know the answer.
- Knowledgeable and brought state-of-the-art research ideas into his lecture. Sharing his own PhD experience was also a nice touch.

AREAS FOR IMPROVEMENT [e.g. inability to answer student questions, deficiencies in content knowledge, absence of examples/irrelevant examples, difficulties with student rapport, etc.]:

- Would be nice to give an outline of the lecture at the start (I realize I should do this more diligently myself).
- Ran slightly overtime.
- Not his fault, but the projection was dark and out-of-focus. The bottom of each slide was hard to read from the back.

ADDITIONAL COMMENTS BEYOND THE LECTURE [e.g. correlation between exam questions and learning objectives, reflection on and incorporation of previous review and suggestions for improvement in teaching, etc.]:

- It's a very good idea to use the class project as a driver for the course. I think it's a great way to engage students in the material.

OVERALL: A very engaging, enthusiastic instructor.

Date of Conference __4/10/12__   Observer Signature __Hao Ling__

Modified 1/2011/PJD

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THE UNIVERSITY OF TEXAS AT AUSTIN
OFFICE OF GRADUATE STUDIES
COMMITTEE REPORT, MASTERS AND DOCTORAL

FOR SUN, NAN

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NAME	EID	LAST SEM	COMM POSITION	MAST OR DOCT	DEGREE	FIELD	YYS	2ND DEGREE	FIELD	YYS
BAUTISTA, HAROLD H.	hhb343	122	CHAIR	M	M.S.E.	ELECTRICAL AN	20122			
BAYOUMY, MOSTAFA ELSAYED	mb42775	139	CHAIR	M	M.S.E.	ELECTRICAL AN	20139			
CHEN, LONG	lc28854	162	CHAIR	D	PH.D.	ELECTRICAL AN	20162			
CHOWDHURY, SK. FAHAD	sfc355	156	MEMBER	D	PH.D.	ELECTRICAL AN	20156			
DOLLO, PHILIPPE MARC	pmd523	162	CHAIR	M	M.S.E.	ELECTRICAL AN	20162			
FONTAINE, ROBERT A.	raf2347	139	CHAIR	M	M.S.E.	ELECTRICAL AN	20139			
FORBES, TRAVIS MICHAEL	tf5274	139	MEMBER	D	PH.D.	ELECTRICAL AN	20139			
GANDARA, MIGUEL FRANCISCO	mfg924	169	CHAIR	M	M.S.E.	ELECTRICAL AN	20129			
GNANA, ANOOSH	ag52276	152	CHAIR	M	M.S.E.	ELECTRICAL AN	20152			
GULATI, PARIDHI	pg22265	162	CHAIR	M	M.S.E.	ELECTRICAL AN	20162			
GUO, WENJUAN	wg3582	162	CHAIR	D	PH.D.	ELECTRICAL AN	20162			
GUPTA, AMIT KUMAR	akg577	142	MEMBER	D	PH.D.	ELECTRICAL AN	20142			
HU, CHENGQING	ch29463	156	MEMBER	D	PH.D.	ELECTRICAL AN	20156			
HUNG, CHENG-HSIEN	ch29537	159	MEMBER	D	PH.D.	ELECTRICAL AN	20159			
JIN, XIANKUN	xj356	139	CHAIR	M	M.S.E.	ELECTRICAL AN	20139			
JUNG, WOO YOUNG	wj2626	149	MEMBER	D	PH.D.	ELECTRICAL AN	20149			
KARDONIK, OLGA	ok666	136	CHAIR	M	M.S.E.	ELECTRICAL AN	20136			
KATRAGADDA, SOWMYA	sk37537	162	CHAIR	M	M.S.E.	ELECTRICAL AN	20162			
KIM, YOUNGCHUN	yk4797	169	MEMBER	D						
KO, JAEGAN	jk27656	169	MEMBER	D						
KOLAR RANGANATHAN, R.	rkr367	169	CO-CHAIR	D						
LEE, HSUN-CHENG	h15869	159	MEMBER	D	PH.D.	ELECTRICAL AN	20159			
LEE, KYOUNGTAE	k123897	132	CHAIR	M	M.S.E.	ELECTRICAL AN	20132			
LU, JINGXUE	j16698	129	MEMBER	D	PH.D.	ELECTRICAL AN	20129			

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PROGRAM GSPBFRP3

THE UNIVERSITY OF TEXAS AT AUSTIN
OFFICE OF GRADUATE STUDIES
COMMITTEE REPORT, MASTERS AND DOCTORAL

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FOR SUN, NAN

NAME	EID	LAST SEM	COMM POSITION	MAST OR DOCT	DEGREE	FIELD	YYS	2ND DEGREE	FIELD	YYS
MA, JI	jm64373	132	CHAIR	M	M.S.E.	ELECTRICAL AN	20132			
MALLORY, DENNIS HENRY	dhm459	132	MEMBER	M	M.S.E.	ELECTRICAL AN	20132			
MASTOVICH, STEFAN NOEL	snm762	129	MEMBER	M	M.S.E.	ELECTRICAL AN	20129			
MISRA, SIDDHARTH	sm43532	156	MEMBER	D	PH.D.	PETROLEUM ENG	20156			
MORENO, MARCO ANTONIO	mm48258	122	CHAIR	M	M.S.E.	ELECTRICAL AN	20122			
MORTAZAVI ZANJANI, S. M.	sm34352	149	MEMBER	D	PH.D.	ELECTRICAL AN	20149			
PAK, JIWOO	jp34493	142	MEMBER	D	PH.D.	ELECTRICAL AN	20142			
PARRISH, KRISTEN NGUYEN	kp8353	136	MEMBER	D	PH.D.	ELECTRICAL AN	20136			
RAFI, ASLAMALI AHMED	aar2246	132	MEMBER	D	PH.D.	ELECTRICAL AN	20132			
RAGAB, KAREEM ABD-ELGHANI	kar2322	166	CO-CHAIR	D	PH.D.	ELECTRICAL AN	20166			
RAHMAN, MD. MANZUR	mr34466	169	CHAIR	D						
REVANNA, NAGARAJA	nr7556	169	MEMBER	M	M.S.E.	ELECTRICAL AN	20142			
SANYAL, ARINDAM	as45744	159	CHAIR	D	PH.D.	ELECTRICAL AN	20159			
SINGH, VINEET KUMAR	vks344	169	MEMBER	D						
TANG, XIYUAN	xt584	149	CHAIR	M	M.S.E.	ELECTRICAL AN	20149			
TENNANT, DANIEL MONCRIEF	dmt965	169	MEMBER	D						
TINTIKAKIS, DIMITRI	dt7596	126	MEMBER	M	M.S.E.	ELECTRICAL AN	20126			
WANG, HUAN	hw5362	139	MEMBER	M	M.S.E.	ELECTRICAL AN	20139			
WANG, PEIJUN	pw5326	142	MEMBER	M	M.S.E.	ELECTRICAL AN	20142			
WANG, YE	yw5692	169	MEMBER	D						
XU, XIAOQING	xx954	169	MEMBER	D						
YADAV, ROHIT	ry2555	169	MEMBER	D						
YANG, SHIXUAN	sy5543	162	MEMBER	D	PH.D.	ENGINEERING M	20162			

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                                COMMITTEE REPORT, MASTERS AND DOCTORAL
                         FOR SUN, NAN

                      LAST   COMM       MAST OR                                            2ND
NAME          EID     SEM    POSITION   DOCT    DEGREE   FIELD           YYS    DEGREE   FIELD     YYS
----------    -----   ----   --------   ------- -------  -----           ----   ------   -----     ---

YOON, YEONAM  yy4285  169    CHAIR      D

YOU, LI       ly3578  142    CHAIR      M       M.S.E.   ELECTRICAL AN   20142

ZHANG, BOYANG bz2355  122    MEMBER     M       M.S.E.   ELECTRICAL AN   20122

ZHANG, WEN    wz2329  126    MEMBER     M       M.S.E.   ELECTRICAL AN   20126
```

List of Postdoctoral Fellows

Nan Sun
Electrical and Computer Engineering
The University of Texas at Austin
nansun@mail.utexas.edu

No Postdoctoral Fellows Supervised.

Budget Council Assessment of Research, Publications and Other Evidence of Scholarship/Creativity for Nan Sun for Promotion from Assistant Professor to Associate Professor

Prepared by Budget Council Members Ranjit Gharpurey and Michael Orshansky

This Research Assessment of Dr. Nan Sun provides an overview of his areas of research interest, publication record, grant record, comments from faculty members and industry experts active in the same or similar areas of research. The assessment utilizes materials provided by the candidate, including his CV and his research statement, and letters of reference provided by external experts.

In summary, Dr. Nan Sun has demonstrated a consistently strong research record. He has made significant advances to the state-of-the-art in the field of analog and mixed-signal IC design, and demonstrated new application spaces for integrated circuit designs. Based on the originality of his research, his publication and funding record, and the opinion of experts in the field, Dr. Nan Sun exceeds the norm for promotion in his field, both at UT and in peer academic institutions.

Research Areas and Contributions

Dr. Nan Sun's research is focused on analog and mixed-signal integrated circuit (IC) design. Within this space, he has made significant original contributions in advanced analog-to-digital conversion techniques, frequency synthesis, low-power analog techniques, time-domain signal processing, and compressive sensing based analog front-ends. These designs are core to multiple communications and consumer applications. It should be noted that this research includes not only a theoretical investigation, but a complete design implementation in commercial CMOS technologies followed by physical performance verification, and the work is benchmarked against advances from other universities and industrial efforts. His work also includes an investigation of IC implementations that can enable new interdisciplinary applications, an example of which is his path-breaking work in miniaturized Nuclear Magnetic Resonance (NMR) systems. His contributions are summarized below.

1. **Contributions to Integrated Circuits and Systems for Emerging Applications (Key Papers J11, J16, J22)**

Nuclear Magnetic Resonance (NMR) has served as a major analytical tool in the life sciences, chemistry and engineering applications. During his Ph.D. at Harvard, Dr. Sun demonstrated an approach for the design of miniaturized Nuclear Magnetic Resonance (NMR) Systems. This remarkable feat of integration reduced a 120-kg commercial NMR system to one that could be held in the palm of the hand. This work led to the scaling of the size and weight by over three orders of magnitude (> 1000 times), and simultaneously increased the sensitivity by a factor of 150, relative to the commercial NMR system. A key to this miniaturization was an optimization of the NMR detector hardware to incorporate a key aspect of NMR physics, namely the highly frequency-selective filtering provided by nuclear spins. Dr. Sun has continued this research at UT, and has in fact received the prestigious NSF CAREER grant for this work, in addition to industrial support.

A second project that deals with emerging IC applications is wearable epidermal electronics. This work is being performed in collaboration with a faculty colleague, Prof. Nanshu Lu, of the Aerospace Engineering and Engineering Mechanics Department in the Cockrell School. The goal of this project is to develop wearable, flexible epidermal electronic sensors for long-term monitoring of biological signals, such as ECG and blood pressure. Dr. Sun's effort is focused on integrating sensor electronics on a single IC platform in order to minimize the form factor of the solution. The IC solutions require investigation of

sensor power management, sensor readout and near-field communication hardware. The research is supported by NSF and NIH, and in a space of two years, has resulted in new low-noise designs with state-of-the-art performance metrics.

2. Contributions to Advanced Analog Circuit Design Techniques in Scaled CMOS Technologies (Key Papers J18, J10, C5, C3)

Dr. Sun's group has established itself as one of the top groups in the nation in the field of deep-submicron CMOS analog IC design. The primary motivation for migrating analog IC design to CMOS has been to leverage the cost-reductions allowed by proliferation of digital ICs, for which there is no alternative technology that is competitive with CMOS. Beyond cost-advantages, however, cutting-edge research in current analog and mixed-signal IC designs seeks to discover design techniques and architectures that provide improved performance by exploiting unique aspects of CMOS, compared to what is achievable in other technologies such as Bipolar or BiCMOS. Dr. Sun's innovative work in this area has followed two broad paradigms of digitally-assisted analog circuit design and time-domain analog signal processing.

Dr. Sun's research utilizes the signal processing capability that is easily available in CMOS to compensate for analog non-idealities. His group's work includes novel digital background calibration techniques, wherein digital adaptive filters are employed to extract analog non-idealities and compensate these in the digital domain. His innovations have led to implementations with significantly lower hardware complexity.

Dr. Sun's group has also gained high visibility through its work on time-domain analog signal processing. This approach relies on the high accuracy that CMOS allows in the time-domain, owing to the very high switching speed of scaled CMOS. Using this approach, his group has recently demonstrated VCO-based Sigma-Delta ADCs with the highest performance figure-of-merit of all VCO-based ADC designs. This work has led to innovations in VCO designs optimized for such ADCs, mismatch-shaping and layout techniques.

3. Contributions to Research in Data Conversion and Fractional-N PLL Techniques (Key Papers J13, C15, C1)

While real-world signals are analog in nature, most signal processing in current communication and sensing systems is performed in the digital domain. This requires analog-to-digital and digital-to-analog converters. The power-dissipation and performance of modern systems is often limited by the capability of these converters, and therefore, advances in these designs can have a major impact on these implementations. It should be noted, that data conversion is one of the most researched areas within the space of analog IC design, and making new contributions in this space is exceedingly challenging, as noted in several of the reference letters. In spite of this, Dr. Sun has made major contributions to the design of ultra-low-power and high-performance successive approximation register (SAR) ADCs. His work addresses a key power bottleneck in the design of low-power SARs, namely the power dissipation for driving switches and the DAC reference. He has utilized statistical estimation techniques to reducing comparator noise, which is another innovation in low-power design. His work has also led to new ADC architectures, that merge the benefits of SAR ADCs with Sigma-Delta ADCs, which allows for using noise shaping to achieve high resolution in SAR ADCs. He has recently applied his research in multibit Sigma-Delta to the design of Fractional-N phase-locked loop designs, which address key performance limitations arising from phase noise and spurious performance.

The work from his research group in this area has addressed another space, namely advanced mismatch shaping techniques. ADCs that use parallelism or multiple signal paths to enhance performance suffer from mismatches in these paths. Dynamic Element Marching techniques have been reported for addressing these performance limitations. The original research from his team has demonstrated techniques to enhance mismatch shaping order, reduce hardware complexity and mitigate errors arising from inter-symbol interference, which has not been addressed in prior work.

4.   Contributions to Analog Architectures for Compressive Sensing (Key Papers C26, C9)

Compressive sensing exploits signal sparsity to reduce hardware requirements. In a collaborative project with Prof. Ahmed Tewfik of the Electrical and Computer Engineering Department, Dr. Sun has demonstrated a power efficient approach for implementing an analog compressive sensing encoder. Specifically, his work has led to techniques that replace OP-AMP based analog integrators in these encoders with switches and capacitors.

It should be highlighted that Dr. Sun has collaborated with three senior faculty members working in digital IC design and signal processing techniques, in addition to his collaboration with faculty in the Aerospace Department. These collaborations are highly encouraged in the Department. The willingness and ability to identify new problem areas and collaborate with experts in complementary areas is essential to cross-disciplinary research and to growing the application space of IC design.

Publication Record

Dr. Sun has an excellent publication record. As an Assistant Professor, he has published 22 Journal Papers and 33 Conference Papers. This work has been published in the top journals for IC design, including the Journal of Solid State Circuits, Transactions on Circuits and Systems-1, Transactions on Circuits and Systems-2, and top-tier conferences, including the European Solid State Circuits Conference and VLSI conference. He is the lead author on 3 book-chapters, and a second-author on 1. A majority of the papers include a full IC-based verification of the proposed architectures and approaches, which is a prerequisite for most circuits journals and conferences. In light of this, the publication record is even more creditable, given that with a new doctoral student, a typical turnaround cycle for a functional, although not necessarily publication-worthy, IC is approximately 1.5-2 years. Furthermore, the above venues are exceedingly competitive, where the acceptance rate can be in the range of 25-35%.

There is an uptick in the publication productivity of Dr. Sun in the second half of his probationary period. One factor that may have impacted this increased publication rate is the revival of the University program for free access to advanced silicon fabrication at the leading IC foundry (TSMC). For reasons having to do with UT-TSMC contract negotiations, this service that was valuable to the candidate's work, was not available from 2011 to June 2013.

His total citations from Google Scholar are 489, with an h-index of 12, which is a strong record in this area, especially at his early stage of career.

The strength of this publication record can be further understood by comparing Dr. Sun's record with those of other recently promoted Associate Professors in his area of research at several Universities with highly reputable IC-design programs.

Faculty	University	Professor Rank	BS	PhD	Tenure Probationary Period				Number of Citations at Promotion	Career H-Index
					Time	Journal	Conf.	Total		
Sudhakar Pamarti	UCLA	Associate	1995	2003	05-10	16	10	26	315*	15
Ada Poon	Stanford	Associate	1996	2004	08-13	13	24	37	680	19
Jeyanandh Paramesh	CMU	Associate	1996	2006	07-12	5	17	22	268*	12
Nan Sun	UT Austin	Assistant	2006	2010	11-16	22	34	56	489	12

*Estimated from Google Scholar

The comparison to peers shows that Dr. Sun's overall publication productivity is outstanding. The total number of citations that his work received also compares well to the citation numbers of his peers at the time of their promotion.

Comments from External Reviewers

Dr. Sun's external reviewers highlight the originality and significance of his work. All reviewers recommend that he be promoted to Associate Professor. Sample comments from the letters are provided below:

Prof. Gabor Temes, NAE, IEEE Life Fellow, Prof. Emeritus, Oregon State University:
"His papers on these topics describe mathematically sophisticated and also practically useful algorithms and circuits. I am sure that they had a wide influence in the field – they certainly impressed and influenced our group here."
"The number of his publications in highly-regards and selective journals and conferences is very high."
"I predict an exceptionally successful future career for him"

Prof. David J. Allstott, Mackay Professor in Residence, UC Berkeley, IEEE Fellow:
"He impressed me with his world-class blend of creativity, analytical abilities, experimental acumen and breadth."
"The quantity of Prof. Sun's production is impressive."
"Prof. Sun also has an excellent record of advising graduate students. It is impressive that he has already graduated 3 Ph.D. with 12 more in the pipeline. It is the unusual breadth of his research that stimulates such a large and capable group of graduate students. It is especially impressive that one of his Ph.D. graduates is a tenure-track Assistant Professor at SUNY Buffalo. Academic jobs in this area are scarce so it is rare and very impressive that he has placed a student in academics already."

Prof. Allstott states that Dr. Sun is of the same caliber as some of his most talented advisees. At the Associate Professor level, he compares them to Prof. Jeyanandh Paramesh and Prof. Nathan Neihart at Carnegie Mellon University and Iowa State University respectively.

Prof. Terri Fiez, IEEE Fellow, Vice Chancellor for Research, University of Colorado:
"Prof. Sun has established a high caliber program that rivals the best at any university … Dr. Sun has found solutions for both dynamic and static errors in multi-element dynamic element matching systems. Something that has eluded researchers around the world. In my research, my graduate students and I have sought out Dr. Sun's publications as critical works from which to build."

Prof. Boris Murmann, IEEE Fellow, Stanford University:
"I view Dr. Sun as one of the most intelligent young researchers in our field. He can clearly drive mixed-signal IC design research into very innovative directions."

Prof. Murmann compares Dr. Sun favorably to Prof. Mike Chen of the University of Southern California, noting that Dr. Sun's accomplishments, while of similar caliber, have been achieved without the benefit of industrial experience.

Prof. Anthony Carusone, Professor, University of Toronto:

"His publication record is top-notch, with articles appearing in the most significant journals in our field."

"What strikes me most about Prof. Sun's work is the breadth of his accomplishments, spanning many of the hottest topics in analog/mixed-signal integrated circuit design."

"He has, in a few years, established his group as a major lab in his field, having international impact. His record, in this regard, is at or near the top of his cohort."

Prof. Ian Galton, IEEE Fellow, University of California, San Diego recommends that the candidate should be promoted, though he expresses some concerns regarding the candidate's publication record. He believes Prof. Sun should publish more in the premier circuits journal, namely the IEEE Journal of Solid State Circuits (JSSC). He opines that "The top journal in his field for presenting IC implementations is the IEEE Journal of Solid-State Circuits (JSSC), yet Professor Sun's only papers in JSSC are those from his PhD work with his advisor.". It is noted that Dr. Sun has several papers in highly competitive conferences, with IC implementations, each of which can potentially lead to papers in JSSC, as stated by Prof. Galton himself. Furthermore, he has two papers submitted to this journal that are in review.

He also states that "The top journal in his field for presenting theoretical results that underlie enhancements for IC implementations is the IEEE Transactions on Circuits and Systems (TCAS) I: Regular Papers, but he has only published three papers in this journal. Instead he has published many such papers in TCAS II: Express Briefs and Electronics Letters, which tend to focus on the fast dissemination of simple ideas that are often incremental in nature."

While TCAS-II does indeed focus on rapid dissemination, the journal is a high-quality peer-reviewed publication that follows all the best IEEE publication practices.

Another concern is with the style of papers. Prof. Galton gives advice for "Professor Sun to write such papers in a more balanced, analytical fashion" pointing out that the papers "sometimes contain sweeping statements, often without proof, about the benefits of his ideas and the drawbacks of previously published techniques."

Prof. Galton's overall assessment of Prof. Sun is positive, i.e., "If he continues on his current path, but follows the advice outlined above, I believe he has the potential to become a top person in his field."

An example of the industrial impact of Dr. Sun's letter is provided by **Dr. Krishnaswamy Nagaraj, IEEE Fellow of Texas Instruments Inc.**

"Dr. Sun has made many highly novel, disruptive contributions to mixed-signal circuits and signal processing."

"Many of these ideas are bound to be adopted by the industry. In fact, these have already inspired new lines of thinking in our own organization in TI."

 "I personally put Dr. Sun's work on par with the work being done in some of the other reputed universities that I regularly interact with, like Columbia University, Oregon State University, and the University of Michigan."

Research Funding and Student Graduation

Dr. Sun's funding record is exemplary and is well-aligned with his current and future research goals. He has received funding from highly-competitive, peer-reviewed sources such as the National Science Foundation and the National Institutes of Health. He is a recipient of the highly prestigious NSF CAREER Award in 2013 for his proposal entitled "Combining Nuclear Magnetic Resonance with IC Technology." During his tenure period as Assistant Professor, he has been awarded 15 grants/contracts as PI, and 17 in total, a rate averaging over 3 per year, which is substantial, especially in a highly competitive area such as circuit design.

He also has an excellent record of industrial funding from companies including Texas Instruments, Cirrus Logic, Intel and Samsung.

His total in-rank funding level is $3.4M, of which his share is $1.7M.

This funding level has enabled him to support a group of 11 PhD students, which is considered a large group in the area of IC design. Equally impressive is the fact that 3 students advised by him have already graduated with their PhDs, including one who has found a faculty position at the State University of New York (SUNY), Buffalo. In addition, one student who was co-advised by him has also graduated this year.

Summary

Dr. Sun has demonstrated an outstanding track record in research. His research is distinguished by its breadth, originality and productivity, and based on the assessment of reviewers, he exceeds the threshold for promotion.

Ranjit Gharpurey and Michael Orshansky

Five Most Significant Publications in Rank

Nan Sun
Electrical and Computer Engineering
The University of Texas at Austin
nansun@mail.utexas.edu

J5.   **Nan Sun**, Tae-Jong Yoon, Hakho Lee, William Andress, Ralph Weissleder, and Donhee Ham, "Palm NMR and one-chip NMR," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 342-352, Jan. 2011.

J8.   **Nan Sun**, "High-order mismatch-shaped segmented multibit delta-sigma DACs with arbitrary unit weights," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 2, pp. 295-304, Feb. 2012.

J10.   **Nan Sun**, "Exploiting process variation and noise in comparators to calibrate interstage gain nonlinearity in pipelined ADCs," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 4, pp. 685-695, Apr. 2012.

J19.   Arindam Sanyal, Long Chen, and **Nan Sun**, "Dynamic element matching with signal-independent element transition rates for multibit delta sigma modulators," *IEEE Transactions on Circuits and Systems - I*, vol. 62, no. 5, pp. 1325-1334, May 2015.

J23.   Kyoungtae Lee, Yeonam Yoon, and **Nan Sun**, "A scaling-friendly low-power small-area delta-sigma ADC with VCO-based integrator and intrinsic mismatch shaping capability," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 561-573, Dec. 2015.

Research Statement for Professor Nan Sun

My research focuses on the design of advanced analog integrated circuits (ICs) for current and emerging applications. Over the past 5 years while in rank, I have made technical contributions to multiple topics and published or had accepted for publication 56 peer-reviewed papers in leading journals (22) and conferences (34), over 90% of which I am the corresponding author.

1. Research Contribution: High-Performance and Ultra-Low-Power Analog IC Design

The motivation to work on core analog IC research is that many fundamental problems remain unsolved. For example, the dynamic switching error remains a key challenge for high-linearity data conversion circuits broadly used in sensing and communication systems. Moreover, as the transistor channel length continuously scales down, there are new design challenges for analog ICs due to increased variation, reduced power supply voltage, and lower transistor gain. Meanwhile, advancements in IC technology open up new opportunities due to increased transistor speed and timing resolution. A new framework of time-domain analog signal processing (ASP) emerges and can outperform the conventional voltage-domain ASP solutions. Furthermore, there are continued strong demands from industry. Emerging applications (e.g., Internet-of-Things, 5G cellular communication, biomedical implant, and wearable sensors) require novel ultralow power and ultrahigh speed analog circuits. All of them call for further research and innovations.

1.1 Advanced Mismatch Shaping Techniques

Mismatch is a major issue for analog circuit design and fabrication, especially in high-linearity analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). While various dynamic element matching (DEM) techniques have been developed to tackle mismatch, there remain important unaddressed problems of the performance and the hardware cost. My PhD student Arindam Sanyal and I developed novel DEM techniques that can increase the mismatch shaping order [1], reduce the vector quantizer hardware complexity [2], and shape segment mismatch errors with arbitrary unit weight [3].

One critical issue that has not been adequately addressed before is the dynamic switching error. Classic DEM techniques cannot address dynamic errors. In fact, they exacerbate dynamic errors by increasing the element transition rate. We have developed several novel DEM techniques that can address both static mismatch and dynamic transition errors. One is based on the minimization of the element transition rate [4]. The other is to maintain a constant transition rate so that dynamic errors can be turned into a signal independent offset. Moreover, it can shape the dynamic error and ensure high linearity even when the input signal is large [5], [6]. As a result, the circuit linearity is substantially improved. Our contribution is well recognized by the research community. It has enabled Dr. Sanyal to become a tenure-track assistant professor at the State University of New York at Buffalo.

1.2 Digitally Assisted Analog Circuits

CMOS scaling has posed great challenges for analog IC design due to reduced supply voltage and transistor gain. A promising way to address them is to use digital signal processing techniques to assist analog circuits. It allows analog circuits to be non-ideal, but then compensates for their nonidealities in the digital domain. This new methodology reduces the analog circuit performance requirement, thereby simplifying the circuit and reducing power. The key problem in this direction is how to design optimum digitally assisted analog circuit topologies and novel signal processing schemes. My PhD student Kareem Ragab and I have developed several novel digital background calibration techniques. Compared to prior works, our techniques have higher performance, lower power, reduced hardware cost, and faster convergence speed. They have important applications in low-power and high-speed analog ICs built in advanced CMOS processes. Our work has been published in [7]–[12] and is under the second round of review in *IEEE Journal Solid-State Circuits* (*JSSC*) [13]. The work has been well-received by industry. Broadcom (a top IC design company) recruited and hired Dr. Ragab a year before his defense.

1.3 Compressive Sensing Based Analog Front-End

The Nyquist sampling theorem has been the gold standard for signal acquisition. It states that for a signal with bandwidth of BW, the ADC conversion rate needs to be at least $2 \times BW$. Recently, researchers

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have developed the compressive sensing (CS) framework that can break the Nyquist sampling theorem if we know that the signal is sparse in a certain domain. This condition is met by many real world signals, such as wireless signals, video signals, audio signals, and biomedical signals. Taking advantage of this property, we can reduce the ADC conversion rate to save power while still capturing all the information. The concept of CS is intriguing, but there is a critical challenge. The required analog CS encoder requires the use of operational amplifier (op-amp) based analog integrators, which are power hungry and scaling incompatible. To solve this problem, my PhD student Wenjuan Guo and I have developed novel CS architectures that use switches and capacitors to realize CS encoders in the discrete-time domain, thereby significantly reducing power and improving performance [14]–[16]. In addition, in collaboration with Prof. Ahmed Tewfik's group, we extended the CS concept to multi-channel ADCs. Our research has important applications for battery-operated devices with tight energy constraints for signal processing and communication. Our work is appreciated by industry. Dr. Guo was awarded a Texas Instruments PhD Fellowship for two consecutive years for her CS research. She joined Intel after graduation.

1.4 Ultra-Low-Power and High-Performance SAR ADC Design

Successive approximation-register (SAR) ADCs are gaining popularity due to their scaling friendliness and low hardware complexity. They consume lower power than $\Delta\Sigma$, pipelined, and flash ADCs especially when the target resolution is below 10 bits. Our research focuses on increasing SAR ADC energy efficiency for ultra-low-power applications such as biomedical implants and wireless sensors. We also invented new architectures that can increase SAR ADC resolution. Our contribution starts with a low-power bidirectional single-side (BSS) switching technique that can reduce both DAC reference and switch driving power [17]–[19]. Compared to the widely used monotonic switching technique, our common mode voltage variation is much smaller and we can freely control the common mode voltage for speed, noise, and offset optimization. We have also developed low-power techniques to reduce comparator noise. Our group, for the first time, brings statistical estimation theory to ADC design. Our basic idea for reducing comparator noise is to repeat the last SAR comparison multiple times, and then, estimate the conversion residue at the comparator input, based on the number of observed '1's or '0's at the comparator output. This technique has low hardware cost, and can greatly improve ADC SNR without significantly increasing comparator power and DAC resolution [20]. The *JSSC* version is in the second round of review [21]. Recently, we invented a new architecture that merges SAR ADC with $\Delta\Sigma$ ADC so that we can use quantization noise shaping to achieve high resolution [22]. $\Delta\Sigma$ modulator is a well-established topic, but prior works require the use of op-amps that are scaling unfriendly and power inefficient. Our new architecture achieves $\Delta\Sigma$ modulation within a SAR ADC framework without the use of an op-amp. Instead, we use only passive switches and capacitors to perform passive integration. We also realize dynamic analog addition and amplification within a low-power comparator. The power and hardware complexity is greatly reduced. In addition, our group have developed new high-speed and low-power SAR ADC architectures using loop unrolling and digital offset mismatch calibration [11], [23], [24]. The PhD student driving our SAR ADC research is Long Chen. He joined Broadcom after graduation.

1.5 Time-Domain (TD) Analog Signal Processing (ASP) Techniques

CMOS scaling makes it hard to follow the classic analog signal processing (ASP) methodology that is heavily based on the use of high-gain op-amps. To address this challenge, a new direction is to perform ASP in the time domain (TD) by taking advantage of the increasing transistor speed. Our group has developed several novel time-domain ASP techniques that are low-power and scaling friendly. We designed a novel dual ring voltage-controlled-oscillator (VCO) based $\Delta\Sigma$ ADC. It not only obviates the need for op-amps, but also has an intrinsic mismatch shaping capability that addresses the DAC mismatch issue [25], [26]. Later on, we came up with novel circuit topologies that further reduce power [27]. We also devised new layout strategies to make them synthesis friendly. Our latest development is a new phase quantizer that doubles the phase linear range and the ADC resolution [28]. The chip achieves the highest Schreier figure-of-merit (FoM) of 174 dB among all existing VCO-based ADCs. We have also developed hybrid ADCs that combine SAR or pipeline with ring VCOs [10], [29]. Our SAR-VCO ADC achieves the highest Walden FoM of 18.5fJ/conversion-step among all existing VCO-based ADCs [30]. Additionally,

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using TD ASP, we have designed a low-power capacitive-to-digital converter (CDC) that achieves the highest power efficiency among prior CDC works [31].

1.6 Reducing Phase-Noise and Spur in $\Delta\Sigma$ Fractional-N Phase-Lock-Loop (PLL)

A critical issue in wideband fractional-N PLL is the quantization noise from its 1-bit $\Delta\Sigma$ modulator. This quantization noise leads to large jitter and phase noise. It also causes fractional spurs. We recently developed a new fractional-N PLL architecture that can substantially reduce both the phase noise and the spur [32]. The key idea is to design a truly multibit frequency divider. To our best knowledge, our group is the first to introduce the mismatch shaping technique in multibit $\Delta\Sigma$ DACs into the field of fractional-N PLL design. It can lower the phase noise and fractional-N spur by 18 dB with our proposed 3-bit $\Delta\Sigma$ modulator and 8-element divider. We envision this new architecture to be widely used in high-accuracy clock generation circuits required by high-speed communication systems.

2. Research Contribution: Combining Nuclear Magnetic Resonance (NMR) with IC Technology

In addition to core analog IC design research, I have also been exploring new application spaces for ICs with the goal of bringing transformative changes to science and technology outside the conventional IC application spaces of computing and communication. One example of my efforts along this direction is the miniaturization of NMR systems. I started this research during my PhD at Harvard and continue working on it at UT. NMR is powerful way to examine the property of a material, and thus, it has a wide array of applications, such as biomolecular sensing, medical imaging, and oil and gas exploration. The benefits of NMR would be broadly available if NMR instruments could be made small and low cost. Nonetheless, NMR systems remain bulky, heavy, and expensive, with their use limited in hospitals, testing facilities, and laboratories. By combining the physics of NMR with CMOS radio-frequency (RF) ICs, I built an entire NMR system in a 0.1 kg platform, which can be held in the palm of the hand [33]–[38]. This system is 1200 times smaller, 1200 times lighter, yet 150 times more spin-mass sensitive than a 120-kg commercial system. Conventional NMR systems are bulky because they use large magnets to produce strong NMR signals. The key to my order-of-magnitude size reduction was to take an approach opposite the convention: I used a very small, ping-pong-ball-size magnet for the system size reduction, and overcame the resulting far weakened NMR signal by designing high-performing CMOS RF ICs that can detect feeble nuclear spin motions. This work is meaningful from several points of view. From the NMR application point of view, the size and cost reduction can amplify the usefulness of NMR in its various applications. From the circuit design point of view, the work showcases how IC chips can be used not only for wireless communication, but also for biosensing aimed at disease detection. From the biosensing viewpoint, it offers a new direction for rapid and low-cost general-purpose diagnostics using hand-held systems. In addition, it has made a commercial impact. My patent has been licensed and served as the foundational technology for a start-up company that raised $13.9M in 2015 [39]. I have also received NSF CAREER award for my proposed research combining NMR with IC design.

3. Newly-Started and Future Research Directions

As the classic analog IC research field is maturing, I plan to venture into new directions and focus more on emerging applications. My future research agenda directly builds upon my past success. I have accumulated abundant experiences working at the intersection of engineering, physics, biology, and medicine. In addition, I have developed solid expertise in analog circuits by solving hard circuit problems. It allows me to address the core challenges in new fields via circuit innovations.

3.1 Wearable Electronics and Non-Invasive Patient Monitoring

A key focus of my future research is wearable electronics. Wearable devices that can transmit information from or to human body are now transforming two prominent fields: mobile health (mHealth) and human-machine interface (HMI). Within the mHealth space, wearable vital sign and physiological sensors can not only track the fitness of our body, but also improve the ability to diagnose and monitor diseases such as seizures, heart arrhythmia, apnea, and movement disorders. Within the HMI space, prosthetic limbs and augmented reality with sensory input to humans are two exemplary applications.

My research aims to address four key challenges in wearable electronics: long-term wearability, high fidelity measurement/stimulation, wireless data/power transmission, and ultralow-power operation. I am

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collaborating with Prof. Nanshu Lu in the Aerospace Engineering and Engineering Mechanics Department. Prof. Lu knows very well the mechanical side of the wearable sensors, while I am the expert on the electrical side. We have received funding from NSF and NIH since 2015.

One of our specific goals is to create novel wearable and flexible epidermal electronic sensors for accurate and long-term monitoring of biological signals, such as ECG, EMG, EEG, blood pressure, and skin hydration. Conventional bio-potential sensors have large motion artifacts. By contrast, our proposed wearable sensor can greatly reduce motion artifacts by forming an intimate contact between the sensor and the human body. Our vision is to make the sensor so small and flexible that it can bend and stretch like skin. There are several critical challenges on the circuit side. We need to fully integrate all the sensor electronics on a single IC chip to minimize the form factor. Its power needs to be ultralow to guarantee long operation time without requiring a bulky battery. Furthermore, we need wireless communication capability so that data can be sent without using wires that are cumbersome and produce motion artifacts. A key design challenge is that since the entire sensor patch is placed on the skin, there are significant loading effects due to the conductive human body. Even worse, this body loading effect is different for every person and changes due to skin stretch and skin hydration level variation. We need to develop novel circuit architectures to constantly monitor and compensate the body loading effects. Although this research topic started just a year ago, we have made significant progress on the ultralow power analog IC design. We have invented a new low-noise amplifier topology that achieves a noise efficiency factor (NEF) of 1.0 via aggressive current re-using. This NEF, which indicates the power efficiency of the circuit, is the best among all existing works according to our best knowledge. Through this research, not only are we expecting exciting new circuits, but also novel sensing systems that can deliver unprecedented high-quality bio-potential signals. There are many applications of the proposed wearable sensors. An important one is non-invasive vital sign monitoring of pre-mature babies in neonatal intensive care unit (NICU). Existing sensors are all wired. They cannot guarantee long-term reliability or high signal fidelity. Prof. Ahmed Tewfik from ECE and Prof. David Paydarfar from Dell Medical School recently established an initiative consisting of multiple faculties to address this critical NICU need. I have been actively participating in this initiative.

3.2 Interactive Analog Synthesis

Design automation of analog circuits is an important but unsolved problem. Unlike digital circuits, analog circuit design is primarily a manual process, leading to low productivity, high design cost, long time-to-market, sub-optimal performance, and high chip failure rate. The technology scaling has made it harder to manually design analog circuits. Device models become increasingly complicated, causing large errors in first-order hand calculations. Furthermore, advanced nanometer processes have large variations. There is not a systematic way to manually optimize yield. Brute-force over-design leads to large penalties in circuit performance and area. We are developing novel interactive analog synthesis tools to address these challenges. Prior analog design automation approaches do not work well because circuit designers are kept out of the loop. The analog synthesis problem is cast as a closed-box optimization problem with hardly any interaction with the designer. As a result, the capability of existing tools is limited, leading to uncompetitive, inconsistent, and unreliable circuit performance. Moreover, because designers are not involved, it causes misunderstanding and mistrust. We propose a different approach. Our goal is to create new analog synthesis tools to empower designers, not to replace them. They will make use of designers' insights to more quickly and robustly converge to the global optimum. Fuzzy logic will be used to capture the natural ambiguity in human instructions. If there are multiple comparable local optima, the algorithm will feed back different solutions and let the designer pick the one that best matches the design intuition and has the highest potential reliability. In case the synthesis tool encounters difficulty in meeting all specifications, the competing specifications will be reported back to the designer. The tool will then assist the designer to figure out the root cause, so that one can address the problem by modifying the circuit topology. In short, the designer will be at the center of the new analog synthesis flow. If successful, our research may revolutionize the way analog circuits are designed. It can greatly increase productivity, leading to reduced design cost, enhanced system capability, shortened time-to-market, and improved reliability. This research has been funded by NSF since 2015 and is in collaboration with Prof. David Pan.

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3.3 Hardware Security and Anti-Counterfeiting

Hardware security has become a critical issue, as IC manufacturing is continuing to move outside of the US, and it is hard to authenticate chips. Recently, Prof. Michael Orshansky and I are collaborating on the design of a strong physically unclonable function (PUF) IC for chip authentication. We developed a novel circuit architecture that can maintain a good statistical property and consume low power. I am also working on the design of true random number generators (TRNGs) for security purpose. Existing TRNGs consume high power or do not have good statistical properties. We came up with a new TRNG architecture that consumes ultralow power and ensures randomness. In addition, I am also developing new methods for analog design obfuscation to increase the difficulty of chip reverse engineering.

4. Research Sustainability

I have raised $3.4M in external research funding with my share being $1.7M. Roughly 70% is from federal agencies (e.g., NSF and NIH) and 30% is from industry (e.g., Texas Instruments and Samsung). I have also raised $0.7M with my share being $0.5M in in-kind donations from silicon foundries (e.g., TSMC). This is a critical enabler for my research in analog IC design, since the chip fabrication cost is a major expense. I have established good relationships with both local and out-of-state companies. Based on my past success in fundraising, I am very confident about the financial sustainability of our group.

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Table 1. Research Summary

Metric	Value
Peer-reviewed journal publications (in rank *and total*)	22 / 26
Peer-reviewed conference proceedings (in rank *and total*)	34 / 37
Number of *journal* papers *in rank* with UT students *as co-authors*	14
Total citations of all publications (career) *from ISI Web of Knowledge*	228
h-index (career) *from ISI Web of Knowledge**	7
Total citations of all publications (career) *from Google Scholar*	489
h-index (career) *from Google Scholar*	12
Total external research funding raised	$3.4M
Total external research funding raised (candidate's share)	$1.7M
Total number of external grants/contracts *awarded*	18
Number of external grants/contracts *awarded* as PI	16

Table 2. External Grants and Contracts Awarded (Total ≈ $3.4M; My Share ≈ $1.7M)

Role of Candidate and Co-Investigators	Title	Agency	Project Total	My Share	Grant Period
PI: Nan Sun David Pan (co-PI)	SHF: Small: Design/Automation for Synthesizable and Scaling Friendly Analog/Mixed-Signal Circuits	NSF	$450K	$225K	2015-2018
PI: Nanshu Lu (Aerospace); co-PI: Nan Sun	Stretchable Planar Antenna Modulated by Integrated Circuit for the Near Field Communication of Epidermal Electrophysiological Sensors	NSF	$380K	$190K	2015-2018
Sub-award PI: Nanshu Lu (Aerospace); Sub-award co-PI: Nan Sun; PI: Katherine Steele (University of Washington)	Ubiquitous rehabilitation to monitor and improve muscle activity and movement after neurologic injury	NIH	$1.5M total, $370K sub-award total	$185K	2015-2019
PI: Nan Sun	CAREER: Combining nuclear magnetic resonance with IC technology	NSF	$400K	$400K	2013-2018
PI: Nan Sun	High temperature LNA design	COSL	$75K	$75K	2015
PI: Nan Sun	Low-power high-speed ADC for CMOS image sensor	Samsung	$100K	$100K	2015
PI: Nan Sun	Multichannel MRI transceiver design	Samsung	$100K	$100K	2014
PI: Nan Sun	Miniature NMR systems for rock and outcrop analysis	Formation Evaluation Industry Consortium	$105K	$105K	2011-2014
PI: Nan Sun	Gift for student design	Texas	$20K	$20K	2011-

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	contest	Instruments			2015
PI: Nan Sun	Gift	Texas Instruments	$60K	$60K	2015
PI: Nan Sun	Gift	Texas Instruments	$60K	$60K	2014
PI: Nan Sun	Gift	Texas Instruments	$60K	$60K	2013
PI: Nan Sun	Gift	Cirrus Logic	$20K	$20K	2016
PI: Nan Sun	Gift	Cirrus Logic	$20K	$20K	2014
PI: Nan Sun	Gift	Cirrus Logic	$20K	$20K	2013
PI: Nan Sun	Gift	Cirrus Logic	$20K	$20K	2012
PI: Nan Sun	Gift	Intel	$18K	$18K	2012
PI: Nan Sun	Gift	Intel	$30K	$30K	2011
TOTAL			**$3.4M**	**$1.7M**	

Table 3. External In-Kind Donations (Total Market Value ≈ $0.7M; My Share ≈ 0.5M)

	Free Integrated Circuit (IC) Fabrication	Company	Donation in Value	Candidate's Share	Year
Lead PI	4 mm^2 free IC fabrication in 130nm	MOSIS	$20K	$10K	2016
Lead PI	Twice 9 mm^2 free IC fabrication in 40nm	TSMC	$180K	$180K	2016
Lead PI	Twice 25 mm^2 free IC fabrication in 180nm	TSMC	$60K	$60K	2016
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	$37.5K	2015
Lead PI	Twice 9 mm^2 free IC fabrication in 40nm	TSMC	$90K	$90K	2015
Lead PI	25 mm^2 free IC fabrication in 180nm	TSMC	$30K	$30K	2015
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	$37.5K	2015
Single PI	1 mm^2 free IC fabrication in 65nm	Texas Instruments	$10K	$10K	2014
Single PI	1 mm^2 free IC fabrication in 65nm	Samsung	$10K	$10K	2014
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	$37.5K	2014
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	$37.5K	2013
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	$37.5K	2012
Total			**$0.7M**	**$0.5M**	

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Division of Labor – Research Projects

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The division of labor for research projects/grants while in rank is provided in the table below. Only collaborative projects are listed (3 of 18). The full list of awarded grants is available in my CV and research statement.

Co-Investigators	Division of Labor	Title	Agency	Project Total	Candidate Share
PI: Nan Sun David Pan (Co-PI) ECE	NS 50% effort, DP 50% effort	SHF: Small: Design/Automation for Synthesizable and Scaling Friendly Analog/Mixed-Signal Circuits	NSF	$450K	$225K
Co-PI: Nan Sun Nanshu Lu (PI) Aerospace	NS 50% effort, NL 50% effort	Stretchable Planar Antenna Modulated by Integrated Circuit (SPAMIC) for the Near Field Communication (NFC) of Epidermal Electrophysiological Sensors (EEPS)	NSF	$380K	$190K
Co-PI: Nan Sun Nanshu Lu (PI) Aerospace	NS 50% effort, NL 50% effort	Ubiquitous rehabilitation to monitor and improve muscle activity and movement after neurologic injury	NIH	$370K (sub-award total)	$185K

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Nan Sun

University of Texas at Austin
integrated circuits, devices, sensors,
biotechnology

Google Scholar

Citation indices	All	Since 2011
Citations	489	432
h-index	12	12
i10-index	15	15

Title 1–20	Cited by	Year
CMOS RF biosensor utilizing nuclear magnetic resonance N Sun, Y Liu, H Lee, R Weissleder, D Ham IEEE Journal of Solid-State Circuits 44 (5), 1629-1643	65	2009
Palm NMR and 1-chip NMR N Sun, TJ Yoon, H Lee, W Andress, R Weissleder, D Ham IEEE Journal of Solid-State Circuits 46 (1), 342-352	51	2011
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CMOS mini nuclear magnetic resonance system and its application for biomolecular sensing Y Liu, N Sun, H Lee, R Weissleder, D Ham 2008 IEEE International Solid-State Circuits Conference-Digest of Technical ...	35	2008
SAR ADC architecture with 98% reduction in switching energy over conventional scheme A Sanyal, N Sun Electronics Letters 49 (4), 1	29	2013
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Exploiting process variation and noise in comparators to calibrate interstage gain nonlinearity in pipelined ADCs N Sun IEEE Transactions on Circuits and Systems I: Regular Papers 59 (4), 685-695	21	2012
Scalable NMR spectroscopy with semiconductor chips D Ha, J Paulsen, N Sun, YQ Song, D Ham Proceedings of the National Academy of Sciences 111 (33), 11955-11960	17	2014
Palm NMR and one-chip NMR N Sun, TJ Yoon, H Lee, W Andress, V Demas, P Prado, R Weissleder, ... 2010 IEEE International Solid-State Circuits Conference-(ISSCC)	15	2010
Multi-channel sparse data conversion with a single analog-to-digital converter Y Kim, W Guo, BV Gowreesunker, N Sun, AH Tewfik IEEE Journal on Emerging and Selected Topics in Circuits and Systems 2 (3 ...	14	2012
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Proceedings of the IEEE 2013 Custom Integrated Circuits Conference, 1-4

High-order mismatch-shaping in multibit DACs N Sun IEEE Transactions on Circuits and Systems II: Express Briefs 58 (6), 346-350	13	2011
Digital background calibration for pipelined ADCs based on comparator decision time quantization K Ragab, L Chen, A Sanyal, N Sun IEEE Transactions on Circuits and Systems II: Express Briefs 62 (5), 456-460	12	2015
An energy-efficient low frequency-dependence switching technique for SAR ADCs A Sanyal, N Sun IEEE Transactions on Circuits and Systems II: Express Briefs 61 (5), 294-298	10	2014
Small NMR biomolecular sensors N Sun, Y Liu, L Qin, H Lee, R Weissleder, D Ham Solid-State Electronics 84, 13-21	10	2013
A hybrid SAR-VCO $\Delta\Sigma$ ADC with first-order noise shaping A Sanyal, K Ragab, L Chen, TR Viswanathan, S Yan, N Sun Proceedings of the IEEE 2014 Custom Integrated Circuits Conference, 1-4	8	2014
Low-complexity high-order vector-based mismatch shaping in multibit$\Delta\Sigma$ ADCs N Sun, P Cao IEEE Trans. Circuits Syst. II 58 (12), 872-876	8	2011
A 24-µW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique L Chen, A Sanyal, J Ma, N Sun European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014-40th, 219-222	7	2014
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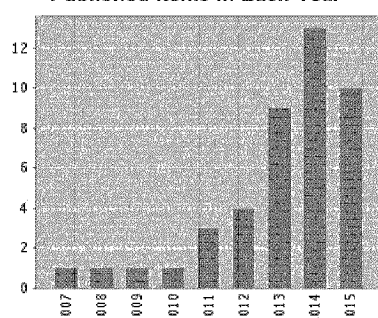
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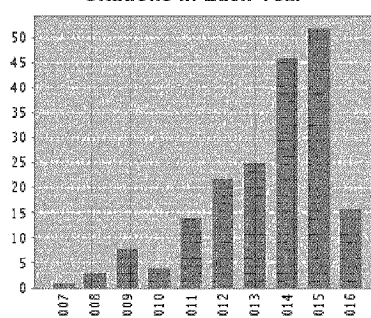
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		By: Sun, Nan; Liu, Yong; Lee, Hakho; et al. Conference: IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Location: Atlanta, GA Date: JUN 15-17, 2008 IEEE JOURNAL OF SOLID-STATE CIRCUITS Volume: 44 Issue: 5 Pages: 1629-1643 Published: MAY 2009	7	8	11	7	1	44	5.50
☐	2.	Palm NMR and 1-Chip NMR							
		By: Sun, Nan; Yoon, Tae-Jong; Lee, Hakho; et al. Conference: International Solid-State Circuits Conference (ISSCC) Location: San Francisco, CA Date: FEB 07-11, 2010 IEEE JOURNAL OF SOLID-STATE CIRCUITS Volume: 46 Issue: 1 Pages: 342-352 Published: JAN 2011	7	5	14	6	2	35	5.83
☐	3.	On the self-generation of electrical soliton pulses							
		By: Ricketts, David S.; Li, Xiaofeng; Sun, Nan; et al. Conference: IEEE Custom Integrated Circuits Conference Location: San Jose, CA Date: SEP 10-13, 2006 Sponsor(s): EEE; IEEE Solid State Circuits Soc; IEEE Elect Devices Soc IEEE JOURNAL OF SOLID-STATE CIRCUITS Volume: 42 Issue: 8 Pages: 1657-1668 Published: AUG 2007	3	2	3	1	0	24	2.40
☐	4.	Exploiting Process Variation and Noise in Comparators to	0	2	3	5	5	15	3.00

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Budget Council Assessment on Academic Advising, Counseling and other Student Services for Faculty Promotion Candidate Dr. Nan Sun

Prepared by Budget Council member David Pan

Introduction

In preparing this assessment, I have used the source material from the candidate's CV, advising statement and other statements, as well as my personal observations of his advising of students. Below, I provide highlights of Assistant Professor Nan Sun's undergraduate and graduate student advising records, which exceed departmental expectations in terms of both quantity and quality.

Undergraduate Student Advising

Dr. Sun has been very involved with undergraduate advising. He has actively participated in undergraduate student mentoring through ECE Open House, IEEE HKN Tech Area Night, undergraduate research, and senior design projects.

It is the expectation in ECE for faculty to be active in advising undergraduate students in their technical area on course selection and career decisions. Dr. Sun has a deep commitment to his advising role and has shown it consistently over the years. He has actively participated in the ECE Open House where he meets with incoming first-year undergraduate students, gives them an overview of the electronic circuit area, and guides them with course selection. He has also regularly represented the Integrated Circuits and Systems area in IEEE HKN Tech Area Night, where he meets with sophomore/junior students and answers their questions on technical area choices, senior and graduate level courses, and provides career advice.

Dr. Sun's advising of undergraduate research and Senior Design teams is outstanding. He actively recruits undergraduate students to join his group for research. So far, he has mentored 6 undergraduate research interns. He trains them individually based on their existing knowledge, and further, assigns his PhD students to interact with them on a daily basis. His undergraduate research advising is fruitful. One of his undergraduate student researchers, Nick Wood, even managed to come up with a novel ADC architecture and publish a first-authored IEEE conference paper, which is very impressive. The senior design teams supervised by Dr. Sun have also been very successful. Since joining UT Austin, he has mentored 5 senior design teams. One of them won the *2nd place* at the year-end ECE Senior Design competition in 2016. Another senior design team was a *top-10 winner nationwide* in the 2013 Texas Instruments (TI) Analog Design Competition.

Graduate Student Advising

Dr. Nan Sun has graduated four (4) PhD students during his appointment as an Assistant Professor at UT Austin, which is remarkable in terms of quantity. Among

them, three graduated under his sole supervision and one under his co-supervision. The quality of Dr. Sun's PhD graduates is also high. For example, Dr. Arindam Sanyal (PhD in 2016 under Dr. Sun's sole supervision) has published 12 first-authored papers at premier journals and conferences, and successfully landed a tenure-track assistant professor position at State University of New York at Buffalo. Dr. Wenjuan Guo (PhD in 2016 under Dr. Sun's sole supervision) received the TI PhD Fellowship for two consecutive years. Dr. Sun's PhD students are well sought after in academia and industry.
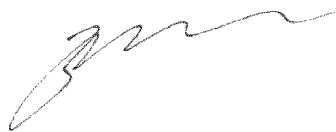
Dr. Sun has also graduated fourteen (14) M.S. students who have chosen the MS thesis or report option. This is a very large number in terms of MS student supervision, and it is a big commitment of Dr. Sun's time and resources. MS students typically only spend two years at school and their first year is just course work. However, Dr. Sun managed to craft proper topics for these students who are constrained by time (one semester for MS report and two semesters for MS thesis). It is impressive to see that under Dr. Sun's supervision, some MS students even managed to publish IEEE journal and conference papers. Dr. Sun's MS students are also well sought after in academia and industry.

Dr. Sun is currently supervising 11 PhD students (including 9 sole-supervised and 2 co-supervised) and 2 MS students at UT Austin. This is considered a large research group in the field of analog integrated circuits design. Thus, he has a very healthy pipeline in terms of future PhD graduates.

In addition, Dr. Sun has supervised a number visiting PhD students and visiting scholars. Through such international collaborations, he expands his UT students' scope in both technical and cultural aspects, as well as builds a pipeline for potential students in the future.

Conclusion
Dr. Nan Sun is an outstanding mentor and advisor, and in great demand from students in our program. He works closely and intimately with his advisees and provides a great deal of inspiration and guidance for them. Both the quality and the quantity of his advising exceed expectations for a junior faculty member of his rank.

David Z. Pan

Statement on Academic Advising, Counseling, and Other Student Services

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1. Advising Undergraduate Students

I view undergraduate advising as a central part of my educational duty. I have volunteered for undergraduate advising events organized by both the ECE department and student organizations. I have actively participated in the ECE Department Open House. During this event, I meet with incoming first-year undergraduate students, give them an overview of the electronic circuit area, and guide them on their course selection. I have also been active in IEEE HKN Tech Core Night, during which I meet with sophomore and junior students and answer their questions about technical core choices. I explain different career path choices to them. From my own experience, I find that many students are unfamiliar with the definition of various types of engineering jobs and the degree or skill sets that are required for different positions (e.g., design, verification, testing, application, and process engineers). As a result, many students make wrong decisions that prevent them from getting their dream jobs after graduation. There is an ongoing trend in the integrated circuit area that almost all high-tech jobs (such as design engineers) now require a master's degree. Thus, if students want to pursue those high-paying high-value jobs, they should prepare for graduate school early on. Mentoring students about career planning is an important faculty role that I am happy to fulfill. The Tech Core Night is a casual come and go event for students. This atmosphere encourages students to freely ask any question regarding technical courses and post college opportunities. Helping students select the right courses, set clear degree goals, and make the right career path choices is very rewarding for me.

I have also been active in mentoring undergraduates that want to do research, and since 2012, I have welcomed undergraduate students to do research in my lab. So far, I have mentored 6 undergraduate research interns. I meet with them biweekly for general research discussion. In addition, I assign PhD student mentors to them so that they can quickly learn how to do research by interacting with their mentors on a daily basis. I train undergraduate students for research by assigning well-defined but challenging research projects. For example, the research project of one of my mentees, Kangjoo Lee, is to study nuclear magnetic resonance (NMR) properties of different oil samples. In order to complete this project, Kangjoo must learn to use a wide range of advanced instruments, including spectrum analyzer, network analyzer, signal generator, and digital oscilloscope. Such training helps students to greatly improve the skills they need to conduct experiments and prepare for their future research. I also train students on the theoretical side. As an example, I gave another undergraduate student, Xi He, the research topic of studying the convergence behavior of a novel digital background timing skew calibration algorithm. He needs to perform extensive statistical calculations. The entire mathematical derivation runs about 10 pages long. Mentored by a PhD student, Xi was able to carry out those challenging derivations and verify them by running numerical simulations, which closely agree with his calculations. A PhD student in our group is currently following up on Xi's research by developing a silicon integrated circuit chip to fully validate Xi's analysis. Another good example is Nick Wood, who is another of my undergraduate mentees. His research is on the design of an analog-to-digital converter (ADC) with prediction capability. This project contains both circuit design and signal processing

components. Under my supervision, Nick came up with a novel ADC architecture that can significantly reduce power. His research led to a *first-authored IEEE conference paper*. Equipped with abundant research training gained while working in our lab, 4 of my undergraduate mentees have been accepted to top graduate programs in the US, including UT Austin, Carnegie Mellon University, and University of Rochester.

I have also been mentoring undergraduate senior design teams since I joined UT Austin. So far, I have mentored 5 senior design teams, totaling 10 semesters of supervision from 2011 to 2016. I meet students every week to help them understand the project goals, challenges, and strategies. I guide them in how to perform extensive literature research and how to break a large project into smaller parts. My senior design teams have been very successful. One team that developed a wireless soil sensing system won *2nd place* at the end of year senior design competition in 2016. Another team developed a low-power handheld bird call recorder that was a *top 10 nationwide* winner in the 2013 Texas Instruments (TI) Analog Design Competition. The entire team and I were invited to TI headquarters in Dallas for the award ceremony.

2. Advising Graduate Students

I love mentoring graduate students that are involved in research. Seeing my graduate students develop innovative solutions to tackle difficult engineering challenges is very rewarding to me. I have graduated 4 PhD students (one co-advised) and 14 master students, with me being the sole advisor. Our research group currently consists of 11 PhD students (two are co-advised) and 2 master students. All of them are on track to complete their degree program.

When I recruit graduate students, I pay special attention to minority and under-represented student groups, such as women and Hispanic students. *I have recruited in total 9 minority graduate students. I have graduated 1 female PhD, 4 female MS, and 3 Hispanic MS students.*

2.1 Advising PhD Students

I enjoy doing challenging research with my PhD students. My mentoring philosophy is to give challenging problems to students and make myself *maximally* available to them whenever they want to have technical discussions with me. This is a challenging task, because as a faculty member, I am always busy with teaching, proposal writing, and service. However, I have always placed student mentoring as a first priority. I feel strongly that timely discussion is very important in helping students make progress with their research. They need immediate feedback, and by providing that to them, they know that I care about their research. Students can come to my office and meet with me even without an appointment. I believe that I have a duty to share my enthusiasm about research and help them develop an understanding of what constitutes good research and what does not. I like to ask tough questions. I prefer not to act as a "boss," but rather as a resource that they can use to accomplish their own research goals. I find that this is the best way to motivate students to pursue their own research. We have both group and individual meetings. Group meetings are for journal club and sharing design techniques. Students are also asked to do presentations in order to develop good communication skills, which I value highly. The way that I mentor students has been working well, as demonstrated by the fact that my PhD students have successfully reached critical milestones. I have already graduated 4 PhD students (1 co-advised), including Arindam Sanyal, Wenjuan Guo, Long Chen, and Kareem Ragab. All of them have made significant research contributions during their PhD pursuits. For example, Arindam has published

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12 *first-author* papers at top journals and conferences. *He has successfully landed a tenure-track assistant professor position at State University of New York at Buffalo* (SUNY Baffalo). He will start in fall 2016. Wenjuan pioneered the efficient hardware realization of a compressive sensing-based analog front-end. *She was awarded the Texas Instruments PhD Fellowship for two consecutive years.* Long introduced, for the first time, the concept of stochastic resonance and statistical estimation to the design of low-power analog-to-digital converters. All of my students have received multiple job offers from top IC design companies. Wenjuan decided to join Intel. Long and Kareem joined Broadcom. Our group has become a target hiring source. Many IC companies consistently invite me to recommend students for job openings.

2.2 Advising Master Students

I always welcome master students to do research in our group. I have supervised 14 master students for their thesis or reports. I place a high standard on their research. Because master students spend only two years on campus and typically need to focus on course work in the first year, they can only concentrate on research for one year. Even though their time is limited, I make sure that over one year of time they can go through a complete integrated circuit design process. They will not only work on architectural level studies, but also transistor level schematic and layout designs. This way, they can receive complete research training and be well prepared for both future industry jobs and PhD research. I carefully craft their research program to make sure their project is innovative and significant, and can be finished before their graduation. As a result, my master students are also able to publish high quality research papers in top research journals and present them at conferences. For example, Kyoungtae Lee designed a novel phase-domain analog-to-digital converter (ADC). He not only finished its design and taped out a silicon chip, but also performed comprehensive lab measurements for his chip. He published 1 first-author journal paper and 1 first-author conference paper. To motivate master students, I promise that if they can come up with novel circuit design techniques and design their chip well, I will sponsor them to do a real silicon tape-out. Note that this is a major financial investment from our group, as each silicon tape-out costs about $10,000. So far, I have sponsored 4 master students to do real chip tape-outs: Kyoungtae Lee, Anoosh Ghana, Sowmya Katragadda, and Paridhi Gulati. Students gain invaluable real-world circuit design experiences, and they are much more enthusiastic about their research project when they will be able to have their own first silicon chip by the end of their master's research.

3.   Advising Visiting Scholars and Visiting PhD Students

In addition to mentoring UT students, I have also been very active in mentoring visiting PhD students and scholars. I have mentored 4 visiting PhDs from China and 1 visiting PhD from Portugal. They typically stay with our group for one or two years. I serve as their overseas co-supervisor, and work with them closely to define their PhD topic. I have also hosted in total 7 visiting scholars. One is from Samsung at Korea, while the other 6 are assistant professors from China. They typically stay for a year to learn how to perform the state-of-the-art circuit research. My lab has always been open to visitors. I consider hosting visiting PhD students and scholars as an important way to promote engineering research activities around the world.

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Table 1. Summary of Academic Advising

Metric	Value
Student organizations advised	--
Undergraduate *researchers* supervised	6
PhD students completed*	3.5 (3 sole advisor)
MS students completed*	14 (14 sole advisor)
PhD students in pipeline (as of 09/2016)*	10 (9 sole advisor)
MS students in pipeline (as of 09/2016)*	2 (2 sole advisor)

*Count a student as 1.0 if sole supervisor and 0.5 if co-supervised.

Table 2. Completed Graduate Students Supervised by Candidate

Student *Name*	Co-Supervisor	Degree	Start Date	Graduation Date	Placement
Arindam Sanyal		PhD	09/2011	11/2015	Tenure-Track Assistant Professor at SUNY Buffalo
Wenjuan Guo		PhD	09/2011	02/2016	Intel
Long Chen		PhD	09/2011	05/2016	Broadcom
Kareem Ragab	Michael Orshansky	PhD	09/2011	07/2016	Broadcom
Marco Moreno		MS	09/2009	05/2012	Emerson
Harold Bautista		MS	09/2010	05/2012	AMD
Miguel Gandara		MS	09/2011	05/2012	PhD student at UT Austin
Alex Fontaine		MS	09/2011	05/2013	Applied Research Laboratories
Shitong Zhao		MS	09/2011	05/2013	Qualcomm
Xiankun Jin		MS	09/2011	05/2013	NXP
Olga Kardonik		MS	09/2011	05/2013	Intel
Kyoungtae Lee		MS	09/2012	05/2014	PhD student at UC Berkeley
Ji Ma		MS	09/2012	05/2014	Qualcomm
You Li		MS	09/2013	05/2015	Oracle
Anoosh Gnana		MS	09/2013	05/2015	Teaching Assistant at McCombs School of Business
Phillippe Dollo		MS	09/2014	05/2016	Texas Instruments
Paridhi Gulati		MS	09/2014	05/2016	Analog Devices
Sowmya Katragadda		MS	09/2014	05/2016	Oracle

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Budget Council Assessment on Service to the University and to the Nation, State and Community for Promotion

Candidate Nan Sun

This statement on service to the university and to the nation, state, and community for Assistant Professor Nan Sun was prepared by Budget Council Member Michael Orshansky. This assessment was prepared based on a review of Dr. Sun's annual reports and personal knowledge of his ECE department activities.

Dr. Sun has made significant service contributions that easily meet expectations for service in the Electrical and Computer Engineering Department, both in the area of Academic Advising, Counseling and other Student Service, as well as in the area of Service to the University and to the Nation, State and Community. These areas will be summarized in the following sections.

I. Academic Advising, Counseling and other Student Services

Prof. Sun has actively served our students through advising, counseling, and other student services. He has been an active contributor to events such as the ECE Department Open House and IEEE HKN Tech Core Night, where he represents the electronics area.

Since 2012, Dr. Sun has served as a member of the ECE Graduate Student Recruiting Committee. This committee is tasked with identifying outstanding applicants and making recommendations for admissions, fellowships, and TA positions. For several years, as part of this committee, Prof. Sun was the organizer of the site visits for the most promising graduate student applicants. There is a great deal of administrative work involved in coordinating this process, and Dr. Sun has tirelessly handled this task very well over the years.

II. Service to the University and to the Nation, State and Community

During his rank as Assistant Professor, Dr. Sun has been a member of a number of committees. At the University level, he served on the Parking and Traffic Appeals Committee. He served on several important Department Committees, including the ECE colloquium committee, the integrated circuits and systems (ICS) area graduate admission committee, the junior faculty search committee, and Silicon Laboratories Endowed Chair

search committee. By all accounts, Dr. Sun is doing an excellent job in serving on these committees.

Dr. Sun also has served on multiple national grant review committees, specifically, he has been very active in serving the National Science Foundation (NSF) proposal review panels. He has served on 4 panels in both the Directorate for Engineering (ENG) and the Directorate for Computer & Information Science & Engineering (CISE). It is very clear that Dr. Sun is recognized and well respected by these funding agencies and technical communities.

Prof. Sun has contributed substantially to the technical community. He has served as Vice Chair for IEEE Central Texas Solid-State-Circuits and Circuits-and-Systems Society Joint Chapter. As part of this initiative, he has organized many workshops and technical seminars given by leading experts. These seminars have benefited the ECE students as well as local professionals. The great work that Prof. Sun has done on behalf of this organization has been recognized by the *Best Chapter of Year Award* from IEEE Circuits-and-Systems Society in 2014. Prof. Sun also has served as an Associate Editor for two publications and on a number of technical program committees.

Dr. Sun's level of service and involvement in the professional community is excellent.

Summary prepared by Budget Council member Michael Orshansky.

Michael Orshansky

Service to the University and to the Nation, State, and Community

Nan Sun
Electrical and Computer Engineering
The University of Texas at Austin
nansun@mail.utexas.edu

1. Service to the University

I have been very active in university services since joining UT in 2011. I view it as an important way for me to contribute to the university.

1.1 Department and Collegiate Committee Service

I have served on the following committees:
- ECE curriculum reform committee since 2016
- ECE colloquium committee since 2015
- ECE integrated circuits and systems (ICS) area graduate admission committee since 2011
- ECE junior faculty search committee since 2015
- ECE Silicon Laboratories Endowed Chair search committee from 2014 to 2015
- University Parking and Traffic Appeals Committee from 2012 to 2014

1.2 Organizer for ECE ICS Seminar Series

Since 2011, I have been the organizer for the ECE ICS seminar series. Over the past 5 years, I have organized over 50 technical talks given by renowned university professors and industry experts. These seminars greatly benefit students and facilitate research collaborations.

1.3 Organizer for Silicon Tape-out Shuttles through MOSIS

Since 2012, I have been the organizer for the integrated circuit research proposal submitted to MOSIS, the multi-project-wafer integrated circuit fabrication service provider. With the contribution from Prof. Jacob Abraham, Prof. Ranjit Gharpurey, and Prof. Michael Orshansky, we have successfully obtained 5 free silicon shuttles using IBM 130nm processes. For each shuttle, the silicon area is shared among several research groups at UT. The total market value for these silicon shuttles is about $320,000. I am the lead writer for the research proposals, the MOSIS account administrator, and the organizer for each tape-out.

1.4 Organizer for Silicon Tape-out Shuttles through TSMC

From 2015 to present, I have been the lead organizer for the silicon tape-out shuttles through Taiwan Semiconductor Manufacturing Company (TSMC). I have set up a close relationship with the TSMC Austin office by visiting them frequently and actively engaging them in the research. Since 2015, TSMC has been willing to support our research with free tape-outs using both 40nm and 180nm CMOS processes. The silicon area is shared among groups that are led by Prof. Jacob

Abraham, Prof. Ranjit Gharpurey, and Prof. TR Viswanathan. In 2015, I arranged one 40nm tape-out and two 180nm tape-outs. In 2016, I will arrange two 40nm tape-outs and two 180nm tape-outs. The market value for these free TSMC tape-outs is about $360,000. While TSMC has stopped their university shuttle program for most universities worldwide, we have been able to secure strong support from TSMC. Under my leadership, the proposed research program from UT has been ranked highly in the TSMC internal review, which is a key enabler for their continued support.

2. Service to the Nation

I have been very active in serving the National Science Foundation (NSF) proposal review panels. So far, I have participated in 4 panels in both the Directorate for Engineering (ENG) and the Directorate for Computer & Information Science & Engineering (CISE).

3. Service to the Technical Community

I have also contributed substantially to the technical community. I have served as Vice Chair for IEEE Central Texas Solid-State-Circuits and Circuits-and-Systems Society Joint Chapter since 2012. I have organized 3 workshops and many technical seminars given by renowned professors and industry experts. These seminars not only benefit students, but also local professionals. Because our IEEE chapter is very active under my leadership, we won the *Best Chapter of Year Award* from IEEE Circuits-and-Systems Society in 2014.

I have been an Associate Editor for two publications since 2016: *IEEE Transactions on Circuits and Systems – I: Regular Papers* and *Journal of Semiconductor*. I have served as a technical program committee (TPC) member of the *IEEE Custom Integrated Circuits Conference* since 2016 and the *IEEE Asian Solid-State Circuits Conference* since 2012. I review papers, organize sessions, and serve as a judge for student design contest.

I have reviewed numerous papers for *IEEE Journal of Solid-State Circuits, IEEE Transactions on Circuits and Systems – I: Regular Papers, IEEE Transactions on Circuits and Systems – II: Express Briefs, IEEE Journal of Emerging and Selected Topics in Circuits and Systems, IEEE Transactions on Biomedical Circuits and Systems*, and *Journal of Nuclear Magnetic Resonance*.

2

**Budget Council Assessment on Honors and other Evidence of Merit or
Recognition for Tenure and Promotion Candidate Professor Nan Sun**

Basis for this Evaluation: This assessment is based on a comprehensive evaluation of the
promotion materials provided by Professor Nan Sun.

The most prestigious honor or award that he received in rank is the National Science
Foundation (NSF) *Career Award* in 2013 for his proposal "Combining nuclear magnetic
resonance with IC technology." This award is given to the top 10% of the proposals
received from Assistant Professors at US institutions after rigorous peer review of their
sole PI proposal by senior faculty members who work in the same field. The NSF Career
Award provides a $400K research grant over a five-year period.

Professor Nan Sun has been very successful in obtaining external funding to build and
sustain his research program. He has attracted $3.4M in external funding of which $1.7M is
his share. The funding comes from diverse and complementary sources, with roughly 70%
from federal agencies and 30% from companies. The federal funding includes the NSF
Career Award, two other peer-reviewed competitive grants from the National Science
Foundation (NSF), and one peer-reviewed competitive grant from the National Institutes of
Health (NIH). The industrial support includes funding from Cirrus Logic, Intel, Samsung
and Texas Instruments. Each company has renewed their funding, which indicates strong
endorsement of Prof. Sun's research program and its impact on analog and mixed-signal
integrated circuit design. Overall, Prof. Sun has developed a balanced funding portfolio. He
has served as the sole PI on all of his industrial projects and on the NSF Career Award. He
has also shown strong collaboration on two of the three NSF grants and on the NIH grant.

Professor Sun's research has a strong experimental component. In particular, he designs,
fabricates and validates ideas in analog and mixed-signal integrated circuits (ICs). He has
received significant in-kind contributions above and beyond the external funding in the
preceding paragraph. The in-kind contributions from MOSIS, Samsung, Texas Instruments
and TSMC have allowed Professor Sun and his graduate students to fabricate 15 analog and
mixed-signal ICs at these leading semiconductor foundries. The estimated market value is
$700K, with his share being $500K.

Professor Sun was elevated to IEEE Senior Member in 2016. With more than 400,000
members, IEEE is the "world's largest technical professional organization dedicated to
advancing technology for the benefit of humanity" (http://www.ieee.org). Elevation to
IEEE Senior Member certifies that Prof. Sun has at least five years of significant
international impact in the field of analog and mixed-signal integrated circuit design.

After joining the faculty at The University of Texas at Austin in January 2011, Prof. Sun
received two prestigious university faculty fellowships:

- Jack Kilby / Texas Instruments Endowed Faculty Fellowship in Computer
  Engineering, 2015-2016
- Fellow of the AMD Chair in Computer Engineering, 2013-present

These awards from The Cockrell School of Engineering recognize his research efforts in analog and mixed-signal IC design.

In summary, Prof. Nan Sun has not only been successful in raising funding to build and sustain a research program, but he is also receiving substantial local, national and international recognition, including as one of the top young stars in his field.

Prepared by the ECE Department Budget Council Member:

Brian L. Evans

Brian L. Evans, PhD
Engineering Foundation Professor
Department of Electrical and Computer Engineering
The University of Texas at Austin

Honors, Merit, and Recognition

Nan Sun
Electrical and Computer Engineering
The University of Texas at Austin
nansun@mail.utexas.edu

1. Research Honors

I am honored to have received the National Science Foundation (NSF) CAREER Award for my research on combining integrated circuit technology with the physics of nuclear magnetic resonance. This research has been featured in the EE Times, MIT Technology Review, R&D Magazine, and Electronics Weekly. Since 2014, I have been Fellow of AMD Endowed Chair in Computer Engineering due to my research on high-performance integrated circuits design. In 2015, I received the ECE Department's Jack Kilby Research Award for my proposed research on phase-domain analog signal processing techniques. In addition, I have also received a UT Austin Summer Research Award for my proposal on neural silicon interface.

2. Research Funding

I have been successful in securing competitive grants, which are enumerated in my Research Statement. In total, I have received 17 grants and contracts, and I am the Principal Investigator for 15 of them. The total funding is about $3.4 million, and my share is about $1.7 million. My government grants come from various sources, including NSF Engineering Directorate, NSF Computer & Information Science & Engineering Directorate, and NIH. They fund a diverse research agenda on integrated circuits and their emerging applications. In addition to government grants, I have also received industry contracts and gifts from leading integrated circuits companies, such as Intel, Samsung, Texas Instruments, and Cirrus Logic. This shows that my research has not only high intellectual value, but also important real-world impacts. In addition, I hold in total 6 patents. One patent has been licensed and served as the foundational technology for a start-up company that raised $13.6 million in Round A fundraising in 2015.

Besides research funding, I have also been successful in raising in-kind donations from semiconductor companies. My research on integrated circuits requires frequent silicon tape-outs, which are very costly. Over the past 4 years, I have obtained 11 free silicon fabrication shuttles whose total market value is over $700K. This external support enables us to perform IC design research in advanced technology nodes. Note that these in-kind donations from companies are also highly competitive in nature. To my best knowledge, there are only 6 universities in the US that are still on the free university shuttle program of the Taiwan Semiconductor Manufacturing Company (TSMC). To get a free shuttle, every proposal has to go through a highly competitive internal review process. The proposals from our group have been consistently highly ranked, which enables us to receive continued support.

3. Invited Talks and Papers

My research has been broadly recognized in both academia and industry. I have been frequently

invited to give research talks. I have delivered in total 50 seminars at leading universities and companies, including Stanford (3 times), Harvard (2 times), Intel Labs, Texas Instruments Kilby Labs, and the IBM T. J. Watson Research Center. I have also published 1 invited journal paper, 2 invited conference papers, and 4 invited book chapters.

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LETTERS RECEIVED – NAN SUN

Name of reviewer, rank or title, department, university	David Allstot MacKay Professor of Residence Department of EECS University of California, Berkeley
Brief statement of expertise and reason for selection*	Expertise: data converters, filters, power amplifiers, sensor interface circuits
Other relevant information**	IEEE Fellow, IEEE CAS Darlington Award, IEEE W.R.G. Baker Award, ISSCC Beatrice Winner Award
Nominated by	Budget Council
Date letter received	July 18, 2016

Name of reviewer, rank or title, department, university	Anthony Chan Carusone Professor The Edward S. Rogers Sr. Department of Electrical and Computer Engineering University of Toronto
Brief statement of expertise and reason for selection*	Expertise: Wireline communications, data converters
Other relevant information**	Past Editor-in-Chief of IEEE Trans. On Circuits and Systems II: Transactions Briefs, Assoc. Editor of IEEE J. Solid-State Circuits, IEEE SSC Society Distinguished Lecturer
Nominated by	Budget Council
Date letter received	July 15, 2016

Name of reviewer, rank or title, department, university	Terri Fiez Vice Chancellor for Research …and Professor of Electrical, Computer and Energy Engineering University of Colorado, Boulder July 27, 2016
Brief statement of expertise and reason for selection*	Expertise: Data converters, filters, sensor interface circuits
Other relevant information**	IEEE Fellow, IEEE SSC Society Distinguished Lecturer, IEEE CAS Society Distinguished Lecturer, Vice Chancellor of Research at UC Boulder
Nominated by	Budget Council
Date letter received	July 27, 2016

Name of reviewer, rank or title, department, university	Michael P. Flynn Professor Electrical Engineering and Computer Science University of Michigan
Brief statement of expertise and reason for selection*	Expertise: Data converters, analog circuit design
Other relevant information**	IEEE Fellow, IEEE SSCS Distinguished Lecturer, Past Editor-in-Chief Journal of Solid State Circuits
Nominated by	Candidate
Date letter received	August 6, 2016

Name of reviewer, rank or title, department, university	Ian Galton Professor Electrical and Computer Engineering University of California, San Diego
Brief statement of expertise and reason for selection*	Expertise: Data converters, filters, clock generation circuits
Other relevant information**	IEEE Fellow, past Editor-in-Chief of IEEE Trans. On Circuits and Systems – II Analog and Digital Signal Processing
Nominated by	Budget Council
Date letter received	July 28, 2016

Name of reviewer, rank or title, department, university	Peter Kinget Bernard J. Lechner Professor of Electrical Engineering Department of Electrical Engineering Columbia University
Brief statement of expertise and reason for selection*	Expertise: RF circuits, ultra-low-voltage circuits
Other relevant information**	IEEE Fellow, IEEE Communications Society Award for Advances in Communication
Nominated by	Budget Council
Date letter received	August 1, 2016

Name of reviewer, rank or title, department, university	Boris Murmann Professor Department of Electrical Engineering Stanford University
Brief statement of expertise and reason for selection*	Expertise: Data converters, filters, sensor interface
Other relevant information**	IEEE Fellow, Friedrich Wilhelm Bessel Research Award, IEEE SSC Society Distinguished Lecturer
Nominated by	Candidate
Date letter received	July 18, 2016

Name of reviewer, rank or title, department, university	Krishnaswamy Nagaraj TI Fellow MCU Division Texas Instruments
Brief statement of expertise and reason for selection*	Expertise: Data converters, filters, power amplifiers, sensor interface circuits
Other relevant information**	TI Fellow, IEEE Fellow, Past Editor-in-Chief of IEEE Journal of Solid-State Circuits
Nominated by	Candidate
Date letter received	July 19, 2016

Name of reviewer, rank or title, department, university	Sudhakar Pamarti Associate Professor Electrical Engineering Department University of California, Los Angeles
Brief statement of expertise and reason for selection*	Expertise: Analog, mixed-signal and RFIC design, signal processing
Other relevant information**	Associate Professor, NSF Career Award
Nominated by	Candidate
Date letter received	July 21, 2016

Name of reviewer, rank or title, department, university	Shanthi Pavan Professor Department of Electrical Engineering Indian Institute of Technology Madras
Brief statement of expertise and reason for selection*	Expertise: Data converters, filters, modulators, sensor interface circuits
Other relevant information**	NAE member of India, past Editor-in-Chief of IEEE Trans. Circuits and Systems I: Regular Papers, IEEE SSC Society Distinguished Lecturer
Nominated by	Candidate
Date letter received	July 24, 2016

Name of reviewer, rank or title, department, university	Edgar Sanchez-Sinencio TI J. Kilby Chair Professor and Director of the Analog and Mixed-Signal Center Department of Electrical and Computer Engineering Texas A&M University August 1, 2016
Brief statement of expertise and reason for selection*	Expertise: Data converters, filters, analog circuit design techniques, DC-to-DC
Other relevant information**	IEEE Fellow, IEEE Darlington Award, IEEE CASS Golden Jubilee Medal, IEEE CASS Distinguished Lecturer, University Distinguished Professor
Nominated by	Budget Council
Date letter received	August 1, 2016

Name of reviewer, rank or title, department, university	Gabor C. Temes Professor School of Electrical Engineering and Computer Science Oregon State University
Brief statement of expertise and reason for selection*	Expertise: Data converters, filters, sensor interface
Other relevant information**	NAE member, IEEE Fellow, IEEE CASS Golden Jubilee Medal, IEEE Gustav R. Kirchhoff Award, IEEE CAS Mac Van
Nominated by	Candidate
Date letter received	July 5, 2016

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
Cockrell School of Engineering

1616 Guadalupe St. • UTA Building, 7th Floor • Austin, Texas 78701
http://www.ece.utexas.edu/

June 21, 2016

Dear Prof. Fiez:

The Department of Electrical and Computer Engineering is considering Dr. Nan Sun for tenure and advancement in rank to the position of associate professor at the University of Texas at Austin. We would appreciate your candid assessment of his scholarly contributions to assist our decision-making process. Excellent teaching is an important criterion for promotion, but our evaluation of teaching is being carried out separately, and we are asking you only for information about his scholarly distinction.

Copies of Dr. Sun's curriculum vitae and several recent papers are posted at the following location. You can access them at: https://www.ece.utexas.edu/promotions/nan-sun-2016 using the following credentials:

Username: sun1
Password: RYus8W

We would appreciate your opinions regarding Dr. Sun's major engineering and/or scientific contributions. In preparing your assessment, please consider the following questions:

1. Do you know Dr. Sun, and if so, for how long and under what circumstances?
2. What are the original, innovative, and/or important contributions that he has made in his field of research? Have his publications influenced the thinking of, or the methods used by, others in your field?
3. How would you assess Dr. Sun's development compared with others in his cohort at research-intensive universities?
4. What is your perspective on Dr. Sun's promise for further professional growth and leadership?

We would be grateful for any additional comments you might have. The more specific you can be in your comments, the more helpful your evaluation will be.

Under the laws of the State of Texas, Dr. Sun has the right to request to see any materials in his personnel file, including your letter. Members of our faculty and internal review committees who see your letter as part of the promotion process will hold the comments you make in confidence, however.

For your comments to receive full consideration, we will need to receive a signed letter from you no later than July 25, 2016. It is not necessary for you to send us a hard copy of your letter, an electronic or scanned version is sufficient, provided your institutional letterhead and your signature are included. In addition, please enclose a copy of a short version of your curriculum vitae (preferably no longer than two pages) or the URL for your web site where we may obtain this information. If you have questions, please call me at the number given on the letterhead.

Thank you for your time and assistance with this important matter. As faculty members, we realize that the amount of time required to do a thoughtful review is considerable.

Sincerely,

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering

List of Materials Sent to Outside Reviewers

Nan Sun
Electrical and Computer Engineering
The University of Texas at Austin

1) CV
2) Five Significant Publications
3) Research Statement
4) Teaching Statement

Five Most Significant Publications in Rank

Nan Sun
Electrical and Computer Engineering
The University of Texas at Austin
nansun@mail.utexas.edu

J5.   **Nan Sun**, Tae-Jong Yoon, Hakho Lee, William Andress, Ralph Weissleder, and Donhee Ham, "Palm NMR and one-chip NMR," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 342-352, Jan. 2011.

J8.   **Nan Sun**, "High-order mismatch-shaped segmented multibit delta-sigma DACs with arbitrary unit weights," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 2, pp. 295-304, Feb. 2012.

J10.   **Nan Sun**, "Exploiting process variation and noise in comparators to calibrate interstage gain nonlinearity in pipelined ADCs," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 4, pp. 685-695, Apr. 2012.

J19.   Arindam Sanyal, Long Chen, and **Nan Sun**, "Dynamic element matching with signal-independent element transition rates for multibit delta sigma modulators," *IEEE Transactions on Circuits and Systems - I*, vol. 62, no. 5, pp. 1325-1334, May 2015.

J23.   Kyoungtae Lee, Yeonam Yoon, and **Nan Sun**, "A scaling-friendly low-power small-area delta-sigma ADC with VCO-based integrator and intrinsic mismatch shaping capability," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 561-573, Dec. 2015.

UNIVERSITY OF CALIFORNIA, BERKELEY

BC

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Department of Electrical Engineering and Computer Sciences
University of California, Berkeley
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July 18, 2016

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Dept. of Electrical and Computer Engineering
The University of Texas
Austin, TX 78701

Re: Prof. Nan Sun—Promotion from Assistant to Associate Professor with Indefinite Tenure

Dear Prof. Tewfik:

I am pleased to provide my assessment and strongest possible support for Dr. Nan Sun for promotion from Assistant to Associate Professor with Indefinite Tenure in the Dept. of Electrical and Computer Engineering. I have known Dr. Sun since Feb. 2010 when his work on a palm-sized NMR was presented at the *IEEE International Solid-State Circuits Conference*, which is the top conference in our field. I have interacted with him frequently and gotten to know him well since I interviewed in your Department about a year ago. He is absolutely first-rate in all respects.

He impressed me with his world-class blend of creativity, analytical capabilities, experimental acumen, and breadth. His NMR work, for example, has combined deep aspects of physics, molecular engineering, signal processing, and analog/mixed-signal IC design. His 2010 *ISSCC* paper, "Palm NMR and one-chip NMR" was visionary, interesting and well executed and presented. Since that time, his work has only gotten even better as he has built his program at UT Austin.

The quantity of Prof. Sun's production is impressive. Many of us evaluate productivity informally based on an expectation of two archival journal papers and four conference papers per year measured over a number of years determined by the Ph.D. graduation year. Prof. Sun received his Ph.D. in 2010 so with 26 archival journal papers and 36 conference papers, he easily exceeds this difficult metric. The quality of his work is also very good as determined by the publication of 3 papers in the *IEEE J. Solid-State Circuits*, which is considered the top journal in our field, 13 papers in the prestigious *IEEE Trans. on Circuits and Systems*, and 3 papers in the *IEEE J. of Emerging Technologies in Circuits and Systems*. His conference publication productivity is also impressive with 2 papers at *ISSCC*, more than 15 papers at *ISCAS*, about 10 papers at *ESSCIRC*, etc.

Prof. Sun also has an excellent record of advising graduate students. It is impressive that he has already graduated 3 Ph.D. with 12 more in the pipeline. It is the unusual breadth of his research that stimulates such a large and capable group of graduate students. It is especially impressive that one of his Ph.D. graduates is a tenure-track Assistant Professor at SUNY Buffalo. Academic jobs in this area are scarce so it is rare and very imipressive that he has placed a student in academics already.

Prof. Sun's teaching record is superb. I attended a seminar he gave at Oregon State University in May 2016. The audience was mostly graduate students and he was able to relate to all of them by stating the problems he was trying to solve, mentioning as appropriate previous work, if any, on the subjects, placing his group's work in the proper context, and sharing his vision about future challenges. It was a superb technical talk.

Prof. Sun's funding record of about $300K/year is good, but not great While there is some evidence of collaboration with senior faculty colleagues, more of this is advisable.

He is of similar caliber to some of the most talented graduate students I have advised in my 30-year academic career including Dr. Jianjun Zhou (Professor of EE at Shanghai Jiao Tong Univ.), Dr. Michael P. Flynn (Professor of EECS at Univ. of Michigan), and Drs. Jeyanandh Paramesh and Nathan Neihart (Associate Professors of ECE at Carnegie Mellon Univ. and Iowa State University, respectively).

I am totally confident that he will continue to excel in teaching, research, and service as he advances towards in his academic career. His record is strong in all respects and his prospects for continued success are unlimited. He has my strongest possible support for promotion to Associate Professor with indefinite tenure.

Sincerely,

David J. Allstot
MacKay Professor in Residence
Department of EECS
University of California
Berkeley, CA 94720

Jilda Gayle

From:	David J. Allstot <allstot@eecs.berkeley.edu>
Sent:	Sunday, July 17, 2016 3:41 PM
To:	Bearden, Carole A
Cc:	Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject:	Allstot Promotion Reference letter - Nan Sun
Attachments:	Sun_071716.pdf

Hi: I have attached my letter of evaluation for Nan. Please confirm receipt.... Dave

On Thu, Jun 23, 2016 at 2:11 PM, Bearden, Carole A <cjjp@mail.utexas.edu> wrote:

Dr. Allstot,

Thank you for agreeing to write a promotion reference letter for Dr. Nan Sun **by July 25, 2016**. Attached is a formal letter from Dr. Tewfik with a login and password to review all documents for Dr. Sun posted on our secure website.

Please let me know if you have any problems reviewing the documents.

Best regards,

Carole

Carole Bearden

Executive Assistant

Electrical and Computer Engineering

The University of Texas at Austin

(512) 471-4540

1

David Allstot

David Allstot
MacKay Professor in Residence
Department of EECS
University of California
Berkley, CA 94720

Email: allstot@eecs.berkeley.edu

University of California, Electrical Eng. and Computer Science,1979, Ph.D.
Oregon State University, Electrical and Computer Engineering, 1974, M.S.E.E.
University of Portland, Engineering Science, 1969, B.S.E.S.

Biosketch

David J. Allstot received the B.S. (1969), M.S. (1974), and Ph.D. (1979) degrees from the Univ. of Portland, Oregon State Univ. and the Univ. of California at Berkeley, respectively. He has held several industrial and academic positions. He was a Professor of Electrical Enginering at the University of Washington from 1999 to 2012. In 2000, he was appointed as the Boeing-Egtvedt Chair Professor of Engineering. He served as Acting Chair and Chair of Electrical Engineering from 2004 to 2007. He has advised more than 100 M.S. and Ph.D. graduates. He served as Editor of the IEEE Transactions on Circuits and Systems, General Co-Chair of the 2002 and 2008 IEEE Intl. Symp. on Circuits and Systems, and as the 2009 President of the IEEE Circuits and Systems Society. He is a Fellow of IEEE.

BC

The Edward S. Rogers Sr. Department
of Electrical & Computer Engineering
UNIVERSITY OF TORONTO

July 15, 2016

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
Austin, Texas   78701

Dear Dr. Tewfik

Subject: Prof. Nan Sun

I am very pleased to write a letter commenting on Prof. Nan Sun. I first became aware of his by work reading and referencing it in the course of my own research on analog/mixed-signal integrated circuit design. I follow his ongoing work with great interest. His publication record is top-notch, with articles appearing in the most significant journals in our field. I was also pleased to meet Prof. Sun at a recent conference and subsequent visit to Austin.

What strikes me most about Prof. Sun's work is the breadth of his accomplishments, spanning many of the hottest topics in analog/mixed-signal integrated circuit design. These include works on ultra low-power analog-to-digital conversion, time-domain signal processing, and analog circuit techniques for nanoscale technologies. In the last category, his work includes methods to address mismatch and nonlinearity in analog circuits by leveraging digital logic. These are methods of growing importance, and his work in this area is very timely. It addresses growing problems in nanoscale CMOS technologies, and is carefully studied by researchers in the field.

Prof. Sun has been extremely productive, both in terms of the number and the quality of publications, numbers of students trained, and research funding attracted. He has, in a few years, established his group as a major lab in his field, having international impact. His record, in this regard, is at or near the top of his cohort. There is also evidence that Prof. Sun makes considerable effort at outreach, giving several external research talks each year and participating in editorial boards. These efforts enhance the impact of his research, and raise the profile of his lab and his institution.

In conversation with him, it is clear that Prof. Sun has a keen grasp of long-term technology trends and a vision identifying research areas of emerging importance such as analog design automation and new computing paradigms. He is poised to pursue these challenges at the head of the pack, and further establish himself as an international research leader. He is well-connected to industry, so his work is certain to be relevant and impactful.

In summary, I would strongly recommend Prof. Sun, and am confident of his ongoing success. I hope this proves useful in your deliberations, and I am at your disposal if I may be of any further assistance.

Sincerely,

Anthony Chan Carusone
Professor
Phone: 416-946-8170
Fax: 416-971-2286
Email: tony.chan.carusone@isl.utoronto.ca

Jilda Gayle

From:	Tony Chan Carusone <tony.chan.carusone@isl.utoronto.ca>
Sent:	Thursday, July 14, 2016 11:17 PM
To:	Bearden, Carole A
Cc:	Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject:	Re: Promotion Reference letter - Nan Sun
Attachments:	NS_promotion_letter.pdf

Dear Carole,

See attached my promotion reference letter for Nan Sun. Please let me know if you require anything further.

Best regards,
Tony

--
Tony Chan Carusone
Professor, Electrical & Computer Engineering, University of Toronto
Integrated Systems Laboratory
isl.utoronto.ca
Office phone: 416-946-8170

On Thu, Jun 23, 2016 at 4:56 PM, Bearden, Carole A <cjjp@mail.utexas.edu> wrote:

Dr. Carusone,

Thank you for agreeing to write a promotion reference letter for Dr. Nan Sun **by July 25, 2016**. Attached is a formal letter from Dr. Tewfik with a login and password to review all documents for Dr. Sun posted on our secure website.

Please let me know if you have any problems reviewing the documents.

Best regards,

Carole

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University of Toronto, Faculty of Applied Science & Engineering
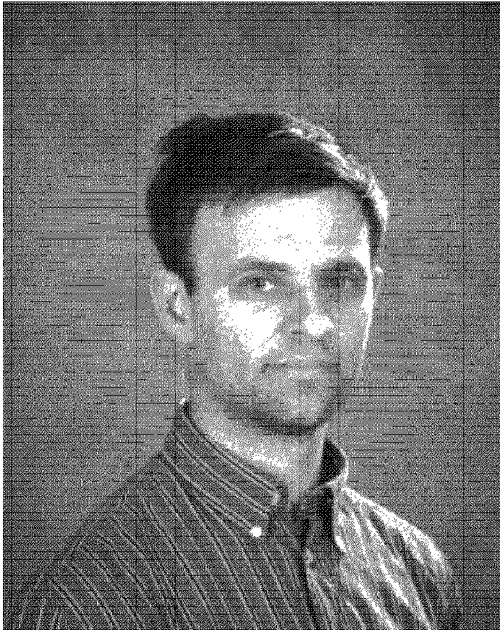
A Chan Carusone

Professor

Electronics

Contact Information
E-Mail: tony.chan.carusone@isl.utoronto.ca
Phone: (416) 946-8170
Office: BA 5134
Website: http://isl.utoronto.ca/

Biography

Tony Chan Carusone completed the B.A.Sc. and Ph.D. degrees at the University of Toronto in 1997 and 2002 respectively. In 2001, he became an Assistant Professor in the Department of Electrical & Computer Engineering at the University of Toronto, was promoted to Associate Professor in 2007, and Professor in 2012. Prof. Chan Carusone is also an occasional consultant to industry, having worked for both large and small semiconductor companies. He researches mixed analog/digital integrated circuit design for signal processing and communication. He co-authored, along with Prof. David Johns and Prof. Ken Martin, the second edition of the classic textbook "Analog Integrated Circuit Design," released in 2011.

Memberships/Awards

- Distinguished Lecturer, IEEE Solid-State Circuits Society
- Editorial Board, IEEE Journal of Solid-State Circuits (2010 – present)
- Editor-in-Chief, IEEE Transactions on Circuits and Systems II: Transactions Briefs, 2009
- Program Committees: International Solid-Sate Circuits Conference, 2011-13; VLSI Circuits Symposium, 2010-2014; Custom Integrated Circuits Conference, 2006-2009
- Best Invited Paper: Custom Integrated Circuits Conference: 2010
- Best Student Paper Awards, co-authorship: European Solid-State Circuits Conference 2014, Custom Integrated Circuits Conference 2011, 2008 & 2007 and Compound Semiconductor Integrated Circuits Symposium, 2005
- NSERC Discovery Accelerator Supplement award, 2011
- Canada Research Chair in Integrated Systems, 2002-2007

BC

University of Colorado Boulder

Terri Fiez, Vice Chancellor for Research
Office of the Vice Chancellor for Research
330 Regent Administrative Center, 26 UCB
Boulder, CO 80309-0026

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July 27, 2016

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering and Chair
Department of Electrical and Computer Engineering
1616 Guadalupe St. UTA Building 7th Floor
Austin, TX 78701

Dear Dr. Tewfik,

I am writing in response to your request for an evaluation of Nan Sun who is being considered for promotion to Associate Professor and granting of indefinite tenure. While I have met Nan at conferences, I don't know him well so my evaluation is based on reading his papers.

Getting right to the point, Professor Sun has established a high caliber program that rivals the best at any university. To graduate 3 Ph.D. students, 13 M.S. students and publish over 20 journal articles and over 30 conference papers is remarkable for this stage in his career. While the numbers are very impressive, I am even more impressed by the quality of his work. His work on small NMR systems is seminal and opens a new field in itself.   To rethink traditional NMR systems and conceive them as small handheld systems is ground breaking work that will continue to have impact over the next decade. His work on analog-to-digital converters (ADCs) is impressive for other reasons. This field is much more mature and requires even more creativity and novel approaches to demonstrate breakthroughs. Many of his papers address the limitations and errors in current ADCs. These problems are well known and many researchers and industry designers have worked on them. In spite of this, Dr. Sun has found solutions for both dynamic and static errors in multi-element dynamic element matching systems. Something that has eluded researchers around the world. He has also tackled the well-studied SAR converter to address several of the fundamental limits and challenges of this architecture. In summary, these publications have served as major advances in the field of analog integrated circuits. In my research, my graduate students and I have sought out Dr. Sun's publications as critical works from which to build.

In your letter you also asked about assessing Dr. Sun's development compared with others at research-intensive universities. Dr. Sun's funding, publications, students graduated are among the very best that I have seen at the top 10-20 universities. This assessment is based on writing letters for other faculty with similar expertise at top 10-20 universities and comparing their records. With the foundation he has built working with students and producing a steady record of innovative research, I am confident that he will develop as one of the top senior researchers/faculty in the field. While I haven't seen him teach, reading his teaching statement, he clearly is passionate about being a first-rate teacher, mentor and researcher. At this point, he is beginning to engage in

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Terri Fiez, Vice Chancellor for Research   Terri.Fiez@colorado.edu
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leadership roles within the professional and I would expect of the next several years, he will
emerge as a critical leader in key conferences and other activities.

Overall, I am extremely impressed with what Dr. Sun has accomplished at this point in his career.
He clearly has earned promotion to Associate Professor and awarding of indefinite tenure. You
should be proud to have him as a member of your faculty. If you have any further questions,
please don't hesitate to contact me.

Sincerely,

Terri Fiez
Vice Chancellor for Research
Professor of Electrical, Computer and Energy Engineering

Nan Sun Letter
Page 2 of 2

Jilda Gayle

From:	Elizabeth Sloan Remnant <Betsy.Remnant@Colorado.EDU>
Sent:	Thursday, July 28, 2016 3:42 PM
To:	cjjp@mail.utexas.edu
Cc:	Tewfik, Ahmed H; Jilda Bolton
Subject:	Promotion Reference letter - Nan Sun
Attachments:	Dr Nan Sun Promotion Reference Letter.pdf; Terri Fiez Bio.pdf

Hello Carole –

Attached please find the reference letter for Dr. Nan Sun from Dr. Terri Fiez, as well as Dr. Fiez's bio.

Please let me know if you have any questions.

Thank you.

Warm regards,

Betsy Remnant
Professional Assistant
Office of the Vice Chancellor for Research
University of Colorado Boulder
330A Regent Administrative Center, 99 UCB
T: 303.735.7505

University of Colorado **Boulder**

print only if necessary

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Terri S. Fiez

Dr. Terri S. Fiez is the Vice Chancellor for Research and Innovation at CU Boulder. Prior to September. 2015, Dr. Fiez was Head of the School of Electrical Engineering and Computer Science at Oregon State University (OSU). In this role, she built strong industry partnerships, grew nationally known research strengths and she was an education serial entrepreneur. In 2008-09 she took a leave of absence from OSU to co-found, launch and serve as CEO of a solar electronics startup company and since then she has helped support several other early stage startup companies. She received her Ph.D. in Electrical and Computer Engineering from Oregon State University and her scholarly interests focus on analog and mixed-signal integrated circuits and novel approaches to innovative education where she has published over 150 papers and advised over 80 graduate students. She was recognized with an NSF Young Investigator, received the 2006 IEEE Educational Activities Board's Innovative Education Award "For Undergraduate Engineering Education Innovation Through Creation and Development of Platforms for Learning® and Its Implementation in the Electrical and Computer Engineering Curriculum through the TekBots® Program" and the 2016 IEEE Undergraduate Teaching Award for the creation of the nation's first online post baccalaureate computer science program. She is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE), has been a distinguished lecturer for the IEEE Circuits and Systems Society and the Solid-State Circuits Society.

C

University of Michigan

Electrical Engineering and Computer Science Building
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(734) 936 2966
mpflynn@umich.edu
www.eecs.umich.edu/~mpflynn

August 6, 2016

To Whom It May Concern:

I have known Dr. Nan Sun, since he was graduate student at Harvard. I became aware of his early work on NMR based sensors. Since then I have followed his career with interest. I met with Dr. Sun and his students during a visit to UT. I also regularly interact with him at conferences and meetings.

Dr. Sun's research has two major threads. Since his graduate research days he has been working on bio-sensing and in particular on NMR based sensors. Concurrently, he has been working on analog-to-digital conversion circuits. His research is now dominated by research on analog-to-digital conversion. His research on both areas is quite successful.

Dr. Sun research on ADCs covers Nyquist and oversampling ADCs, with an emphasis on energy efficiency. Some of this work is on improved noise-shaping ADCs such as on dynamic element matching and reduction of DAC ISI. Much of the work in on energy efficient successive approximation (SAR) ADCs. He has especially applied and improved techniques to improve the energy efficiency and performance of SAR ADCs. For example, this includes the use and improvement of noise-shaping in a SAR ADC, the introduction of modified switching techniques for SAR DAC arrays, and the improvement of use of multiple comparator sampling to reduce errors and noise. He has also worked extensively on voltage-controlled-oscillator (VCO) based SAR ADCs, demonstrating some nice improvements to the VCO ADC approach. This research on ADCs has led to solid results. His ADC work has also led to several publications, for example he had paper in the 2016 VLSI Symposium on Circuits (one of the premier IC design conferences) and he has 6 papers in the upcoming 2016 the European Solid-State Circuits conference (ESSCIRC - a highly regarded conference on circuit design).

Dr. Sun has published 26 journal papers and 36 conference papers. This rate of publication is good for someone working on integrated circuit design at this career stage. In particular, the number of journal papers is high. He has 4 papers in the premier circuit design journal (IEEE JSSC), with 3 of these related to his graduate work. He has 3 papers in the very well regarded, IEEE TCAS I, and several papers in the also good, IEEE TCAS II. From his

conference papers, he has two papers from his graduate work in ISSCC, the premier circuit-design conference and one recent paper in the excellent VLSI Symposium on Circuits as well as several papers in strong conferences such as CICC and ESSCIRC.

Prof. Sun has built a strong circuits group at UT. With over $1.7 million, his research is well funded. He has secured the prestigious NSF Early Career Award. He also has an impressive amount of collaboration with industry, which is critically important for success and impact in this research area. He also has successful collaborations with several colleagues at UT.

Dr. Sun has a very good track record of service both within UT and to the wider community. He is Associate Editor of two IEEE journals including TCAS I. He serves on the Technical Program Committee of ASSCC, which is the top Asian conference on circuit design He also has played a significant role in the IEEE Central Texas Solid-State-Circuits Society and Circuits and Systems Society Chapters. For example, he played a major role in the chapters' guest lecture programs, bringing in top speakers in circuit design to both UT and the Austin IC design community.

Dr. Sun teaches four courses on circuit design at UT. He is an enthusiastic and accomplished teacher and has enhanced his classes with design prizes and interaction with industry. His teaching scores are very strong.

Dr. Sung has built an impressive circuit research group at UT. He is a strong researcher and has a good track record of publication. His research group is well funded. He is a highly dedicated and accomplished teacher. I very strongly support Prof. Sun's promotion to Associate Professor with tenure at UT.

Sincerely

Michael P. Flynn
Professor, EECS

Jilda Gayle

From:	Tewfik, Ahmed H <tewfik@austin.utexas.edu>
Sent:	Saturday, August 6, 2016 3:56 PM
To:	Jilda Gayle; Bearden, Carole A
Subject:	Fwd: Action needed: please let me know by 6/22 if you can provide a reference letter for Nan Sun's promotion in late July
Attachments:	NanSun.pdf; Untitled attachment 00053.htm
Signed By:	tewfik@austin.utexas.edu

regards
Ahmed

_____

Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
1616 Guadalupe St.
UTA 7.416
Austin, TX 78701
USA

Direct: (512) 471-6179
tewfik@austin.utexas.edu

Begin forwarded message:

> **Resent-From:** <tewfik@austin.utexas.edu>
> **From:** Michael Flynn <mpflynn@umich.edu>
> **Date:** August 6, 2016 at 11:35:57 PM GMT+3
> **To:** "Tewfik, Ahmed H" <tewfik@austin.utexas.edu>
> **Subject: Re: Action needed: please let me know by 6/22 if you can provide a reference letter for Nan Sun's promotion in late July**
>
> Hi Ahmed,
> I have attached a letter.
> All the best,
> Mike

1

Flynn Research Group Member

Michael P. Flynn

Email: mpflynn@umich.edu
Office: 2417-F EECS Building
Telephone: 734-936-2966
Website: http://www.eecs.umich.edu/~mpflynn/index.html

Biography
Dr. Flynn joined the University of Michigan in 2001, and is currently Professor. His technical interests are in data conversion, gigabit serial transceivers, and RF circuits. Michael P. Flynn was born in Cork, Ireland. He received the Ph.D. degree from Carnegie Mellon University in 1995. From 1998 to 1991, he was with the National Microelectronics Research Centre, Cork. He was with National Semiconductor in Santa Clara, CA, from 1993 to 1995. From 1995 to 1997 he was a Member of Technical Staff at Texas Instruments, DSP R&D lab, Dallas, TX. From 1997 to 2001, he was with Parthus Technologies, Cork.

Michael Flynn is a 2008 Guggenheim Fellow. He received the 2011 Education Excellence Award and the 2010 College of Engineering Ted Kennedy Family Team Excellence Award from the College from Engineering at the University of Michigan. He received the 2005-2006 Outstanding Achievement Award from the Department of Electrical Engineering and Computer Science at the University of Michigan. He received the NSF Early Career Award in 2004. He received the 1992-93 IEEE Solid-State Circuits Pre-doctoral Fellowship. He is an Associate Editor of the IEEE Journal of Solid State Circuits (JSSC) and serves on the Technical Program Committees of the International Solid State Circuits Conference (ISSCC) and the Symposium on VLSI Circuits. He formerly served on the program committee of the Asian Solid-State Circuits Conference was Associate Editor of the IEEE Transactions on Circuits and Systems II from 2002 to 2004.

BC

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Professor Ian Galton
Electrical & Computer Engineering
University of California, San Diego
La Jolla, California 92093-0407

July 28, 2016

Professor Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
Austin, Texas 78701

Dear Professor Tewfik,

I am providing this letter in response to your June 21, 2016 request for my assessment of Professor Nan Sun's scholarly contributions to date. I was familiar with some of Professor Sun's published work prior to your request, and have since learned more from reading his Research Statement, Teaching Statement, and several additional papers from his group.

Professor Sun's research interests are broadly within the field of CMOS mixed-signal integrated circuits (ICs). The breadth of his work within this field is impressive given the relatively short duration of his career to date. For his PhD work he developed CMOS ICs to monitor nuclear spin for miniature nuclear magnetic resonance systems. It is not clear whether the resolution offered by his approach will be sufficient for commercial deployment, but the work is interesting. Since then, Professor Sun has branched out into digital calibration algorithms to measure and correct analog errors in mixed-signal ICs such as pipelined ADCs, mismatch-shaping DAC architectures that address both unit element mismatches and inter-symbol-interference (ISI), modified SAR and VCO-based ADC architectures, and compressive sensing techniques for ADCs. Most of these latter areas are of significant practical interest, and good ideas in these areas are likely to see significant commercial deployment. Moreover, each of these latter areas are unrelated to Professor Sun's PhD advisor, so it is clear that Professor Sun has successfully made the requisite jump from PhD student researcher to fully independent principal researcher.

Several of Professor Sun's papers propose new enhancements and modifications of well-known circuits such as different types of data converters. For example, in an up-coming ESSCIRC paper his group has proposed an interesting way of performing capacitance to digital conversion by combining prior SAR and VCO-based ADC techniques. As another example, his group has developed extensions of well-known work by others on mismatch-shaping DACs and ISI suppression that involve creativity and appear to offer significant advantages.

It is important to recognize that the enhancements proposed by Professor Sun's group are in a very mature field and many apply to well-established, well-known architectures. Furthermore, the field is highly competitive, with numerous prolific research groups in both academe and industry. People in the field tend to be skeptical of new ideas, so to gain traction (or even get published) new ideas must be demonstrated in working ICs, which adds significant extra complexity to running a research group in the field. These aspects of the field make it very difficult to innovate meaningfully, so it is laudable that Professor Sun has managed to make multiple contributions to date.

One concern I have about Professor Sun's research record, though, is where he has chosen to publish his journal papers. The top journal in his field for presenting IC implementations is the IEEE Journal of Solid-State Circuits (JSSC), yet Professor Sun's only papers in JSSC are those from his PhD work with his advisor. The top journal in his field for presenting theoretical results that underly enhancements for IC implementations is the IEEE Transactions on Circuits and Systems (TCAS) I: Regular Papers, but he has only published three papers in this journal. Instead he has published many such papers in TCAS II: Express Briefs and Electronics Letters, which tend to focus on the fast dissemination of simple ideas that are often incremental in nature. He has also published some longer papers in journals that are less well-known in the field, so they are likely to have less impact than if they had been published in TCAS I: Regular Papers.

It is possible that Professor Sun's choice of journal paper venues is a result of poor advice he has received. I can imagine people telling him that he needs to have as many journal papers as possible to gain tenure, and that venues such as TCAS II: Express Briefs and Electronics Letters offer relatively easy paths to this goal. I would advise Professor Sun to instead focus on writing a smaller number of longer, more substantial papers that thoroughly analyze his ideas. Otherwise, the rate at which Professor Sun's ideas will be adopted by others could be relatively low.

I would also advise Professor Sun to write such papers in a more balanced, analytical fashion. Many of his papers contain good ideas, but they sometimes contain sweeping statements, often without proof, about the benefits of his ideas and the drawbacks of previously published techniques. They also sometimes contain interesting observations about properties of his techniques, but the observations are often stated in passing, again without any real analytical justification. I suspect many of the observations are true, but it is difficult for readers to assess what is known to be true by Professor Sun and what is just conjecture. For example, Paper J19 is riddled with such statements, yet it is a very interesting paper. It could have been greatly improved with a more thorough and quantitative analysis to support its claims of superiority.

In all other respects Professor Sun is doing very well. In addition to my positive observations above about the creativity and diversity of his research, he runs a large research group, and appears to have ample funding. Judging from his student evaluations, he is a gifted and highly-appreciated teacher.

On the whole, I believe that Professor Sun should be promoted with tenure despite the concerns I raised above about his publication choices. He has numerous recently presented and upcoming accepted conference papers that each present an interesting IC implementation, and

that each could potentially be turned into a future JSSC paper. In fact, if he had done this and applied for tenure next year, I think he would have had a much stronger case. Either way, I think it would be a shame not to give him tenure. If he continues on his current path, but follows the advice outlined above, I believe he has the potential to become a top person in his field.

Sincerely,

Ian Galton

Jilda Gayle

From:	Galton, Ian <galton@ucsd.edu>
Sent:	Thursday, July 28, 2016 12:57 PM
To:	Bearden, Carole A
Cc:	Galton, Ian; Galton, Ian; Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject:	Re: Promotion Reference letter - Nan Sun
Attachments:	Nan_Sun_UT_Austin.pdf

Hi Ahmed and Carole,

My letter is attached. Feel free to contact me if you have any questions or need anything else.

In the mean time, I have a question for you. I noticed your cover letter mentions that under Texas law Professor Sun has the right to see my letter if he requests access. I'm assuming that if this happens the version he'll see will be without my name on it. Is this correct?

Regards,

Ian

On Jun 23, 2016, at 2:56 PM, Bearden, Carole A <cjjp@mail.utexas.edu> wrote:

Dr. Galton,

Thank you for agreeing to write a promotion reference letter for Dr. Nan Sun **by August 1, 2016**. Attached is a formal letter from Dr. Tewfik with a login and password to review all documents for Dr. Sun posted on our secure website.

Please let me know if you have any problems reviewing the documents.

Best regards,

Carole

Carole Bearden
Executive Assistant
Electrical and Computer Engineering
The University of Texas at Austin
(512) 471-4540

What starts here changes the world

<Reference letter - Sun-Galton.pdf>

1

Ian A. Galton

University of California, San Diego

Professor, Electrical and Computer Engineering

Faculty-Affiliate, Calit2

Data converters, frequency synthesizers, clock-recovery systems, digital signal processing (DSP) techniques to mitigate the effects of non-ideal analog circuit behavior in mixed-signal integrated circuits (ICs) implemented in CMOS (silicon chips).

Ian Galton manages the Integrated Signal Processing Group at UCSD. The group's research objective is to generate enabling technology for highly integrated, low-cost, communication systems. The research involves the invention, development, analysis, and CMOS integrated circuit implementation of key communication system blocks such as data converters, frequency synthesizers, and clock recovery systems. The emphasis of the research is on the development of digital signal processing techniques to mitigate the effects of non-ideal analog circuit behavior in mixed-signal (combined analog and digital) integrated circuits. The resulting circuits tend to blur the traditionally sharp analog-digital dividing lines in communication systems in order to reduce the precision requirements of the analog circuitry.

Capsule Bio:

Ian Galton received the Sc.B. degree from Brown University in 1984, and the M.S. and Ph.D. degrees from the California Institute of Technology in 1989 and 1992, respectively, all in electrical engineering. Since 1996 he has been a professor of electrical engineering at the University of California, San Diego where he teaches and conducts research in the field of mixed-signal integrated circuits and systems for communications. Prior to 1996 he was with UC Irvine, and prior to 1989 he was with Acuson and Mead Data Central. His research involves the invention, analysis, and integrated circuit implementation of critical communication system blocks such as data converters, frequency synthesizers, and clock recovery systems. In addition to his academic research, he regularly consults at several semiconductor companies and teaches industry-oriented short courses on the design of mixed-signal integrated circuits. He is a Fellow of the IEEE, and has served on a corporate Board of Directors, on several corporate Technical Advisory Boards, as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, as a member of the IEEE Solid-State Circuits Society Administrative Committee, as a member of the IEEE Circuits and Systems Society Board of Governors, as a member of the IEEE International Solid-State Circuits Conference Technical Program Committee, and as a member of the IEEE Solid-State Circuits Society Distinguished Lecturer Program.

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

BC

DEPARTMENT OF ELECTRICAL ENGINEERING

New York, August 1st, 2016

Re: Evaluation for the Tenure Promotion of Nan Sun at U.T. Austin

Dear Promotion Review Committee:

I am writing this letter to strongly recommend Nan Sun for promotion to Associate Professor at your institution.

My biographical details are summarized at the end of this letter. My field of research overlaps significantly with Nan's although that recently I have been more active in radio-frequency IC design and a bit less in mixed-signal IC design. Nevertheless, I feel qualified to provide you an evaluation of his record.

I am currently on sabbatical for which I have taken on a couple of non-academic assignments that are keeping me very busy. I am also writing this letter while traveling so excuse me for the delay and relative brevity. It should not reflect negatively on Nan's evaluation.

I have met Nan several times when I visited the department of Electrical Engineering at your university and at conferences in our field. We have always had engaging conversations and he comes across as a very solid researcher. I have not heard him speak, but in his dossier I read about his passion for teaching and his teaching evaluation scores indeed indicate that his teaching is appreciated by the students.

He has a large research group of 12 current Ph.D. students. Three students have completed their Ph.D. under his supervision, which is a nice achievement for a tenure evaluation time of only 5 years. He has a good mix of funding from federal grants and industrial support. The latter is important in our research field since a good connection with industry gives students access to internships and later employment but also keeps the research critically grounded in practical aspects of design requirements.

Nan's research as a faculty member has primarily focused on mixed-signal design techniques exploiting digital signal processing to enhance or compensate impairments or errors in the analog circuits. His research is tackling relevant problems in building highly efficient analog-to-digital converters and interfaces that are compatible with semiconductor process scaling. His work includes prototyping these techniques in integrated circuits. This is an essential step, but also a costly and time-consuming step. Going from theoretical idea, through circuit realization, simulation, layout and tape-out, and finally to experimental evaluation in the lab can easily take 1.5 years for one trial. Additionally, taking into account the logistics --- fabrication funding, testing lab, computer tools, industrial connections --- of setting up a research group in this field, five years go by very quickly and give a short run-time for tenure promotion. Nevertheless, Nan has succeeded in realizing a substantial body of work. As importantly, he has shown a substantial and consistent growth in his research productivity. The number of papers from his group is growing year by year. Just looking at the recent numbers, six papers at the upcoming ESSCIRC is outstanding and four papers at the 2015 CICC is also remarkable, keeping in mind that all these papers do include experimental chip results.

His publication record is substantial and his group's journal publications have so far mainly focused on the IEEE Circuits & Systems Society Transactions even though many of his papers do include experimental chip results. I am confident that with his current publication activity in the IEEE Solid-State Circuits Conferences we will also see his students publish in the IEEE Journal of Solid-State Circuits in the near future.

Nan's research statement and new grants indicate that he is launching a number of important new research activities. In combination with his research and teaching accomplishments achieved in the past five years, I am confident that he will continue to grow his profile and establish his prominence in the solid-state circuit design research community.

1300 Seeley W. Mudd   Mail Code 4712   500 West 120th Street   New York, NY 10027   Tel. 212-854-3105   Fax 212-932-9421

In closing, I strongly support Nan's promotion to Associate Professor with Tenure. If you have any questions, do not hesitate to contact me at the number below or at peter.kinget@columbia.edu.

Yours,

Peter Kinget
Bernard J. Lechner Professor of Electrical Engineering
+1-212-854-0309

1300 Seeley W. Mudd   Mail Code 4712   500 West 120th Street New York, NY 10027 Tel. 212-854-3105 Fax 212-932-9421

Jilda Gayle

From:	Peter R. Kinget <peter.kinget@columbia.edu>
Sent:	Monday, August 1, 2016 4:04 AM
To:	Bearden, Carole A
Cc:	Ahmed H Tewfik; Jilda Bolton (jildagayle@gmail.com)
Subject:	Re: Promotion Reference letter - Nan Sun
Attachments:	Kinget_20160801_2.pdf; Untitled attachment 00025.htm

Apologies, something strange happened in the PDF conversion. Please use the attached version instead. Best, —
Peter

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Peter R. Kinget received the engineering degree (Summa cum Laude) in electrical and mechanical engineering and the Ph.D. (Summa cum Laude with Congratulations of the Jury) in electrical engineering from the Katholieke Universiteit Leuven, Belgium, in 1990 and 1996, respectively.

From 1991 to 1995, he received a graduate fellowship from the Belgian National Fund for Scientific Research (NFWO) to work as a Research Assistant at the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven. From 1996 to 1999 he was at Bell Laboratories, Lucent Technologies, in Murray Hill, NJ, as a Member of Technical Staff in the Design Principles Department. From 1999 to 2002 he held various technical and management positions in IC design and development at Broadcom, CeLight and MultiLink. In 2002 he joined the faculty of the Department of Electrical Engineering, Columbia University, NY, where currently is the Bernard J. Lechner Professor of Electrical Engineering. He is also a consulting expert on patent litigation and a technical consultant to industry.

His research interests are in analog, RF and power integrated circuits and the applications they enable in communications, sensing, and power management. He is widely published in journals and conferences, has co-authored 3 books and holds 22 US patents with several applications under review. His research group has received funding from the National Science Foundation, the Semiconductor Research Corporation, Department of Energy (ARPA-E), Department of Defense (DARPA), and an IBM Faculty Award. It has further received in-kind and grant support from several of the major semiconductor companies.

Dr. Kinget is a Fellow of the IEEE. He is an elected member of the IEEE Solid-State Circuits Society Adcom, the society's governing board (2011-2013 & 2014-2016), and a member of the Board of the Armstrong Memorial Research Foundation. He is a "Distinguished Lecturer" for the IEEE Solid-State Circuits Society and has been an Associate Editor of the IEEE Journal of Solid State Circuits (2003-2007) and the IEEE Transactions on Circuits and Systems II (2008-2009). He has served as a member of the Technical Program Committee of the IEEE Custom Integrated Circuits Conference (CICC) (2000-2005), the Symposium on VLSI Circuits (2003-2006), the European Solid-State Circuits Conference (2005-2010), and the International Solid-State Circuits Conference (2005-2012).

He is a co-recipient of the "Best Student Paper Award - 1st Place" at the 2008 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, of the "First Prize" in the 2009 Vodafone Americas Foundation Wireless Innovation Challenge, of the "Best Student Demo Award" at the 2011 ACM Conference on Embedded Networked Sensor Systems (ACM SenSys), of the "2011 IEEE Communications Society Award for Advances in Communication" for an outstanding paper in any IEEE Communications Society publication in the past 15 years, of the "First Prize ($100K)" in the 2012 Interdigital Innovation Challenge (I2C), and of the "Best Student Paper Award – 2nd Place" at the 2015 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium.

Personal Website: http://www.ee.columbia.edu/~kinget

Research Group's Website: http://www.cisl.columbia.edu/kinget_group

C

Stanford University   DEPARTMENT OF ELECTRICAL ENGINEERING

July 25, 2016

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering Chairman
Department of Electrical and Computer Engineering
The University of Texas at Austin

Reference Letter: Prof. Nan Sun

Dear Professor Tewfik:

I am pleased to hear that Nan Sun is being considered for tenure and I am happy provide my strong endorsement for this promotion. I will frame my input using the specific categories that you have provided:

1. Do you know Dr. Sun, and if so, for how long and under what circumstances?

I first met Nan Sun in 2009, when he was still a PhD student at Harvard. Nan had been working on digitally calibrated A/D converters that were similar to some of my previous work and we therefore started a conversation. He had identified one of the weak points of my architecture and proposed a new calibration algorithm that converged significantly faster. I was deeply impressed at the time, especially given that he was working on multiple projects in parallel (ADCs, mini NMR systems, soliton experiments, etc.). I have been in touch with him since then and we regularly meet at conferences. Dr. Sun visited Stanford recently to give a seminar talk, which made me aware of his most recent projects and contributions.

2. What are the original, innovative, and/or important contributions that he has made in his field of research? Have his publications influenced the thinking of, or the methods used by, others in your field?

Dr. Sun has made a variety of significant contributions in the design of mixed-signal interface and clock generation circuits. Within my area of expertise, the most important works are related to the design of fast background calibration algorithms (C5, C30, J10 and J20, listed in his CV), the advancement of mismatch shaping in oversampling converters (J22 and J23), as well as extensions to the successive approximation register (SAR) converter architecture (C23, C31, C33, J25, and others).

   The background calibration work contains unique and new ideas that have brought these algorithms from an academic curiosity to a state that is now much more applicable to actual products. I expect that this line of work will draw many citations in the future, once it has been fully digested by the community. The work on mismatch shaping is a rigorous extension of prior art techniques, and substantially improves the performance of the techniques that are in use today. I was especially impressed with the core of the work described in J22, and I look forward to its experimental validation. Much of the other notable work in data converters centers around improving the SAR ADC topology, which is a hot topic at all leading conferences. Here, Dr. Sun's group has published a number of creative ideas, incorporating time-based circuits, compressed sensing, noise estimation, low-energy switching schemes, and a modified loop-unrolled approach.

Stanford University

In the above-discussed areas of research, I think that Dr. Sun achieved a very good balance between quantity and quality in his publications. Moreover, I feel that he has in fact done as well as is possible in shaping up new ideas in the data converter space, and many people in the community are therefore well aware of Dr. Sun's work. However, a concern with this general area of research is that it is clearly maturing, and future work is bound to run into diminishing returns. With this in mind, I would have expected a more direct explanation in the research statement on where he will take this work and what will be next. He describes slivers of interesting new directions toward the end the statement (e.g. analog neuromorphic computing), but it is not clear if he plans on pushing these ideas strongly.

3. How would you assess Dr. Sun's development compared with others in his cohort at research-intensive universities?

A good point of comparison is Mike Chen, who currently up for tenure at USC and is working in the same field. My impression is that Dr. Sun and Dr. Chen have had approximately the same output (quantity and quality) and have earned a similarly good reputation in our community. Since Dr. Chen spent some time in the industry before returning to academia, and I therefore view this outcome as favorable for Dr. Sun, who is still very young and has lots of room to grow in all dimensions (BS completed only 10 years ago!).

4. What is your perspective on Dr. Sun's promise for further professional growth and leadership?

I view Dr. Sun as one of the most intelligent young researchers in our field. He can clearly drive mixed-signal IC design research into very innovative directions and he has shown good productivity in many sub-areas of our field. It is worth noting that this has become incredibly difficult at a time when the prior-art is already very advanced and the competion from industrial researchers is very strong.

What is critical for him at this stage is whether he will find new trajectories for the decades to come, and as the semiconductor field is maturing further. As already mentioned, I would have liked to see a more explicit discussion of this point in his research statement (and also in his seminar talk), but I do not see this as a significant problem for the tenure decision. This might be a good point to be taken up by Dr. Sun's faculty mentor.

In summary, I am happy to conclude that Dr. Sun has become an internationally known expert and "rising star" in the fields of circuits and systems and solid-state circuits. Given the breadth of Dr. Sun's abilities, I expect that he will have an outstanding career as a tenured faculty member in your department and I therefore recommend tenure without any reservations. Please do not hesitate to contact me in case I can be of further help in your evaluation.

Sincerely,

Boris Murmann
Professor of Electrical Engineering, Stanford University
IEEE Fellow

Jilda Gayle

From:	Bearden, Carole A <cjjp@mail.utexas.edu>
Sent:	Thursday, July 28, 2016 8:47 AM
To:	Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject:	FW: Promotion Reference letter - Nan Sun
Attachments:	sun_letter_murmann.pdf; murmann_cv201607_short_acad.pdf

Ahmed and Jilda,

Here is a letter for Nan.

Cheers,

Carole

From: Boris Murmann [mailto:murmann@stanford.edu]
Sent: Wednesday, July 27, 2016 8:39 PM
To: Bearden, Carole A <cjjp@mail.utexas.edu>
Subject: RE: Promotion Reference letter - Nan Sun

Dear Carole,

Attached is my letter.

Regards,
Boris

From: Bearden, Carole A [mailto:cjjp@mail.utexas.edu]
Sent: Thursday, June 23, 2016 2:01 PM
To: Boris Murmann <murmann@stanford.edu>
Cc: Tewfik, Ahmed H <tewfik@austin.utexas.edu>; Jilda Bolton (jildagayle@gmail.com) <jildagayle@gmail.com>
Subject: Promotion Reference letter - Nan Sun

Dr. Murmann,

Thank you for agreeing to write a promotion reference letter for Dr. Nan Sun **by July 25, 2016.** Attached is a formal letter from Dr. Tewfik with a login and password to review all documents for Dr. Sun posted on our secure website.

Please let me know if you have any problems reviewing the documents.

Best regards,

Carole

Carole Bearden
Executive Assistant
Electrical and Computer Engineering

1

Boris Murmann
351 Olmsted Road
Stanford, CA 94305
murmann@stanford.edu
web.stanford.edu/~murmann

EDUCATION

Ph.D. in Electrical Engineering	**2003**
University of California, Berkeley, CA	
Thesis: "Digital Calibration for Low-Power High-Performance A/D Conversion"	
M.S. in Electrical Engineering	**1999**
Santa Clara University, Santa Clara, CA	
Honors: Degree awarded "with Distinction"	
Dipl.-Ing (FH) in Communications Engineering	**1994**
Fachhochschule of the German Telekom, Dieburg, Germany	
Thesis: "Computer Controlled Measurement System for Quality Control in Digital Radio Links"	

EMPLOYMENT AND ACADEMIC APPOINTMENTS

Professor of Electrical Engineering	**2015 – present**
Stanford University, Stanford, CA	
Associate Professor of Electrical Engineering	**2010 – 2015**
Stanford University, Stanford, CA	
Visiting Associate Professor	**2015**
Pierre and Marie Curie University, Paris, France (Prof. A. Baschirotto)	
Visiting Associate Professor	**2011 – 2012**
University of Milan-Bicocca, Italy (Prof. A. Baschirotto)	
Visiting Assistant Professor	**2009**
University of Freiburg, Germany (Prof. Y. Manoli)	
Assistant Professor of Electrical Engineering	**2004 – 2010**
Stanford University, Stanford, CA	
Integrated Circuit Design Engineer	**1999**
R&E International, King of Prussia, PA	
Integrated Circuit Design Engineer	**1994 – 1997**
Neutron GmbH, Hanau, Germany	

TECHNICAL ADVISORY BOARD MEMBERSHIPS

Cephasonics, Santa Clara, CA	**2012 – present**
Redpine Signals, San Jose, CA	**2011 – present**
Totic, Inc., Santa Clara, CA	**2016 – present**
Ikanos, Fremont, CA	**2011 – 2015**
Alvand Technologies, Santa Clara, CA	**2011 – 2012**
Arda Technologies, Mountain View, CA	**2009 – 2012**
Texas Instruments, Dallas, TX	**2008 – 2011**
Samplify Systems, Campbell, CA	**2007 – 2011**

PROFESSIONAL ACTIVITIES & AFFILIATIONS

Program Vice-Chair/Chair, International Solid-State Circuits Conference (ISSCC)	**2015 – 2017**
Technical Program Committee, European Solid-State Circuits Conference (ESSCIRC)	**2011 – 2014**
Technical Program Committee, International Solid-State Circuits Conference (ISSCC)	**2006 – 2015**

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Chair, ISSCC Data Converter Subcommittee	**2012 – 2015**
Selection Committee, ISSCC Student Research Preview	**2008 – 2011**
Associate Editor, IEEE Journal of Solid-State Circuits	**2010 – 2015**
Guest Editor, IEEE Journal of Solid-State Circuits	**2009**
Session Chair, International Conference on Sampling Theory and Applications	**2011**
Session Chair, ISSCC High Speed Data Converter Session	**2009, 2013**
Session Chair, ISSCC Student Research Preview Session	**2008, 2010**
Guest Editor, EURASIP Journal on Advances in Signal Processing, Special Issue	**2007**
Doctoral Dissertation Committees	
- University of Stuttgart, Germany	**2015, 2016**
- University of Ulm, Germany	**2014**
- University of Pavia, Italy	**2012**
- ETH Zurich, Switzerland	**2012, 2013**
- UPMC Paris, France	**2013, 2016**
- University of Macau, China	**2011**
- Vrije Universiteit Brussels, Belgium	**2009, 2010**
- University of Freiburg, Germany	**2009**
- Graz University of Technology, Austria	**2009**

AWARDS AND HONORS

IEEE Fellow	**2015**
Friedrich Wilhelm Bessel Research Award	**2012**
Distinguished Lecturer of the IEEE Solid-State Circuits Society	**2011 – 2012**
Sony Faculty Scholarship	**2010**
Agilent Early Career Professor Award	**2009**
IEEE Custom Integrated Circuits Conference 2008 Best Invited Paper Award	**2008**
VSLI Circuit Symposium Best Student Paper Award	**2008**
ISSCC Outstanding Special-Topic Evening Award	**2008**
Meritorious Paper Award, Government Microcircuit & Critical Technology Conf.	**2005**
Robert N. Noyce Faculty Scholar, Stanford University	**2004 – 2005**
Stanford University Presidential Research Grant for Junior Faculty	**2004**
Stanford Office of Technology Licensing Seed Grant Award	**2004**
Publication ranked in Most-Read Articles of IEEE Journal of Solid-State Circuits	**2003**
Cal VIEW Award for Excellence in Distance Education, UC Berkeley	**2003**
Analog Devices Outstanding Student Designer Award	**2000**
EECS Outstanding Graduate Student Instructor, UC Berkeley	**1999**
German Telekom Scholarship	**1990 – 1994**

PUBLICATIONS

See: http://web.stanford.edu/~murmann

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C

TEXAS INSTRUMENTS

Krishnaswamy Nagaraj

TI Fellow, MCU Division

July 19, 2016

Dr. Ahmed Tewfik

Chairman, Dept. of Electrical and Computer Engineering

UT Austin

Dear Dr. Tewfik,

I am writing this in support of Dr. Nan Sun's tenure and advancement.

I have had the pleasure of knowing him for the past five years. He interacts regularly with multiple groups including ours within TI. We are constantly following the research work in his group. There is a very large overlap between his research area and my organization's interests.

Dr. Sun has made many highly novel, disruptive contributions to mixed-signal circuits and signal processing. I will name a few which have captured our attention

1) **DEM scheme for handling static and dynamic errors in current mode DAC's:** This addresses a very important problem in high speed multi-bit Sigma-Delta ADC's as well as communication DACs. The technique provides high-pass shaping for both ISI and static mismatch. An important application for which we are considering this scheme is in the high speed DAC for a Power Line Carrier (PLC) transmitter

2) **Several innovations in SAR ADC's:** This class of ADC's is the backbone of MCU's and Wireless SOC's. Dr. Sun's group has produced a slew of novel ideas to address a variety of things like switching energy, mismatch calibration, fast convergence, very high speed (700 MS/s!). These ideas are all very practical and useful for the industry. There are 4 papers SAR ADC papers from his group in ESSCIRC 2016. That is impressive by any measure

3) **VCO based ADC's:** This is a rapidly expanding research area. I myself have had a deep involvement with this, having jointly supervised the research work of Dr. Amit Gupta who graduated from UT Austin a few years ago. Here again, Dr. Sun's research spans a broad spectrum. One of his recent papers on this topic is a 250 MSPS, 2 MHz VCO based ADC to be

published in ESSCIRC 2016. The specs for this are very similar to an opamp based ADC that we recently designed for a key product in the same process node. The VCO based ADC consumes less than 1/3 the power consumed by our ADC!

4) **Multi-channel ADC:** Dr. Sun recently conceived of a revolutionary technique that takes advantage of the sparseness of communication channels to enable A/D conversion of multiple channels using a single SAR ADC. He has demonstrated this concept through an actual implementation.

5) **NMR Spectroscopy:** Prof. Sun's PH.D work was on NMR, which is an unusual topic for analog circuits. He is still chipping away at this, with a publication as recently as in 2014. This will help in making NMR spectroscopy more portable, thus opening it up to a large number of new applications.

All of the above speak to the broad spectrum of Prof. Sun's research contributions. Many of these ideas are bound to be adopted by the industry. In fact, these have already inspired new lines of thinking in our own organization in TI. The fact that most of these have been proven in silicon (often in process nodes that we use frequently), makes them even more attractive to us. I also value his willingness to explore new frontiers. Here in the industry we don't usually have the luxury to do that.

I personally put Dr. Sun's work on par with the work being done in some of the other reputed universities that I regularly interact with, like Columbia University , Oregon State University and the University of Michigan. I think that he is very valuable asset for UT Austin. I look forward to collaborating with him in the future.

I extend my whole-hearted support for his promotion.

Regards,

Krishnaswamy Nagaraj

July 19, 2019

Jilda Gayle

From:	Nagaraj, Krishnasawamy <nagaraj@ti.com>
Sent:	Friday, July 22, 2016 2:05 PM
To:	Bearden, Carole A
Cc:	Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject:	RE: Promotion Reference letter - Nan Sun
Attachments:	Recommendation for Nan Sun.pdf; Krishnaswamy Nagaraj Biography.docx

Hello Carole,

I am attaching my recommendation letter as well as a short biography. Please let me know if you need anything else.

Regards,

Krishnaswamy Nagaraj

From: Bearden, Carole A [mailto:cjjp@mail.utexas.edu]
Sent: Friday, June 24, 2016 11:28 AM
To: Nagaraj, Krishnasawamy
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: RE: Promotion Reference letter - Nan Sun

Dr. Nagaraj,

When login into our system please use Sun03. For some reason Sun3 does not work properly.

Many thanks,

Carole

From: Bearden, Carole A
Sent: Thursday, June 23, 2016 3:55 PM
To: 'nagaraj@ti.com' <nagaraj@ti.com>
Cc: Tewfik, Ahmed H (tewfik@austin.utexas.edu) <tewfik@austin.utexas.edu>; Jilda Bolton (jildagayle@gmail.com)
<jildagayle@gmail.com>
Subject: Promotion Reference letter - Nan Sun

Dr. Nagaraj,

Thank you for agreeing to write a promotion reference letter for Dr. Nan Sun **by July 25, 2016**. Attached is a formal letter from Dr. Tewfik with a login and password to review all documents for Dr. Sun posted on our secure website.

Please let me know if you have any problems reviewing the documents.

Best regards,

Carole

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Krishnaswamy Nagaraj

Krishnaswamy Nagaraj is presently with the Microcontrollers Division of Texas Instruments in Dallas, Texas. In this capacity, he is leading architecture and design of mixed-signal circuits for a broad range of applications. Prior to this he has worked with the Analog and Wireless divisions of the company. He was with the Bell Laboratories in Murray Hill, NJ, during 1986-1996, and the University of Waterloo, Ontario, Canada, during 1985-1986.

He has been an Associate Editor of the IEEE Journal of Solid State Circuits and the IEEE Transactions on Circuits and Systems, II and was the Editor-in-Chief of the IEEE Journal of Solid State Circuits during 2004-2007. He was an Adjunct Associate Professor at UPENN during 1998-2004. He is an IEEE Fellow and Texas Instruments Fellow.

C

UNIVERSITY OF CALIFORNIA, LOS ANGELES   UCLA

BERKELEY · DAVIS · IRVINE · MERCED · LOS ANGELES · RIVERSIDE · SAN DIEGO · SAN FRANCISCO   SANTA BARBARA · SANTA CRUZ

SUDHAKAR PAMARTI   ELECTRICAL ENGINEERING DEPARTMENT
ASSOCIATE PROFESSOR   THE HENRY SAMUELI SCHOOL OF ENGINEERING
6731F BOELTER HALL   AND APPLIED SCIENCE
PHONE: (310) 825 2657, FAX: (310) 825 8282   BOX 951594
E-MAIL: SPAMARTI@EE.UCLA.EDU   LOS ANGELES, CALIFORNIA 90095-1594

July 21, 2016

Dear Prof. Tewfik,

Re: Proposed Promotion of Dr. Nan Sun to Associate Professor

It is with enthusiasm that I write this letter in support of Prof. Nan Sun's proposed promotio to Associate Professor with tenure. I have known Prof. Nan Sun mainly through his work and have met him in person only recently.

Prof. Nan Sun works in the area of analog/mixed-signal/RF integrated circuit (IC) design for communciations and other applications. This area is important as such ICs are critical enablers in the development of consumer electronics, electrical communications, and biomedical electronics. The design of such ICs presents a formidable challenge especially in the face of ever stringent performance and power consumption demands anmanufacturing process variability.

Analog/mixed-signal/RF IC design is an established discipline where traditionally researchers employed clever circuit topologies and meticulous design optimization to achieve desired performance goals. Over the last decade, the abundance of cheap digital computational capability (stemming from IC fabrication process technology scaling) has prompted researchers to develop so-called "digitally-assisted" techniques which digital circuits are employed to compensate for analog circuit impairments.

Prof. Nan Sun's research is following this general trend and rather successfully, in my opinion. More importantly, Prof. Nan Sun's research demonstrates a deeper understanding of the capabilities and the role digital-assistance can play in the further development of analog/mied-signal/RF circuits. Unlike most researchers in this field who primarily employ a handful of techniques such as digital calibration or LMS (least mean square) based adaptation to an increasingly larger set of analog/RF circuits, Prof. Nan Sun is bringing advanced statistical signal processing knowledge and considerable mathematical rigour in modeling and subsequently compensating for analog impairments.

While not necessarily original, this approach had resulted in important contributions to his field. Prof. Nan Sun's work on dynamic element matching (DEM) techniques for continuous time digital-to-analog converters (DACs) is a case in point. He has developed/employed sophisticated signal processing techniques such vector quantization and noise shaping to eliminate almost all deleterious effects of static and dynamic errors caused by inevitable mismatches and errors in IC fabrication. Prof. Nan Sun's work in improving the performance of several kinds of analog-to-digital converters (ADCs) is also in the same theme.

Prof. Nan Sun's approach of employing sophisticated digital signal processing technques is extremely powerful and has great potential. Furthermore, his students will be trained in the dual disciplines of IC design and digital

signal processing making them highly valuable to the industry and academia. His publication and funding record so far is proof enough of the value of such research.

Please note that Prof. Nan Sun's PhD research has focused almost exclusively on traditional analog/RF circuit design albeit for a very interesting nuclear magnetic resonance based sensor. In contrast, his subsequent research has overwhelmingly focused on digitally assisted techniques. His PhD advisor doesn't work on this field generally. His long record of publications and successful fund raising in a field that is new to him is demonstrative of his abilities to establish and sustain an independent research program.

For a comparitive evaluation, I would consider Prof. Mike Chen, Prof. Antonio Liscidini, Prof. Nima Maghari, all of whom work on digitally-assisted IC design, and are the best in their career-level. Please note that Prof. Liscidini and Prof. Chen have had more prior work/research experience. Both in publication record and the quality of research undertaken, Prof. Nan Sun is comparable to the first two of this cohort, and is better than Prof. Maghari.

Overall, I am confident that Prof. Nan Sun will grow into an excellent career with significant impact on his field.

Sincerely,

Sudhakar Pamarti

Jilda Gayle

From:	SUDHAKAR PAMARTI <spamarti@ucla.edu>
Sent:	Friday, July 29, 2016 3:36 AM
To:	Tewfik, Ahmed H
Cc:	jildagayle@gmail.com; Bearden, Carole A
Subject:	Re: Action needed: please let me know by 6/22 if you can provide a reference letter for Nan Sun's promotion in late July
Attachments:	Nan_Sun_Tenure_Reference_2016.pdf

Dear Ahmed,

Please find attached my reference letter.

Do let me know if you need the original hard copy as well.

Sudhakar

On Mon, Jul 25, 2016 at 12:51 AM, Tewfik, Ahmed H <tewfik@austin.utexas.edu> wrote:
Dear Sudhakar

That should be fine. Please send us the letter by the end of this week.

regards
Ahmed

Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
1616 Guadalupe St.
UTA 7.416
Austin, TX 78701
USA

Direct: (512) 471-6179
tewfik@austin.utexas.edu

On Jul 25, 2016, at 7:47 AM, SUDHAKAR PAMARTI <spamarti@ucla.edu> wrote:

Dear Ahmed,

I am not done with the reference letter yet. May I take a few more days?

Regards,
Sudhakar

1

UCLA
Electrical Engineering Department
Sudhakar Pamarti
Associate Professor
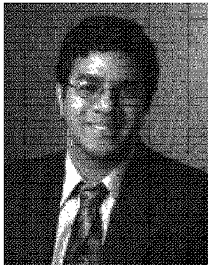
Contact Information
Rm 6731F, Boelter Hall
Electrical Engineering Department
University of California
Los Angeles, CA 90095-1594

Phone: (310) 825 2657

Education
Ph.D., 2003,
Electrical Engineering,
University of California, San Diego

Courses Taught
- EE 110
  Circuit Analysis II
- EE 115C
  Digital Electronic Circuits
- EE 215E
  Signaling and Synchronization
- EE 115B
  Analog Electronic Circuits II

Keywords
mixed-signal, delta-sigma, fractional-N,
phase locked loop, data converter

Biography
Sudhakar Pamarti received his Ph.D. degrees in electrical engineering from the University of California at San Diego 2003. Prior to joining UCLA in 2005, he worked with Rambus Inc. developing high speed chip-to-chip electrical communication interfaces.

Research
Dr. Pamarti is interested in wireless and wireline communication system hardware, particularly in mixed signal circuits blocks such as data converters, frequency synthesizers, and clock synchronization and signal equalization circuits.

His group focuses on developing digital signal processing and communication theoretic techniques to improve the performance metrics of error-prone mixed signal circuitry. He emphasizes both the in-silicon verification and the theoretical analysis of such techniques. Typical research employs delta-sigma modulation for data conversion, frequency synthesis and power amplification; or, using CDMA for Gb/s chip-to-chip communication.

Selected Awards/Recognitions

- NSF Career, 2009.

Sample Publications

- S. Pamarti, L. Jansson, and I. Galton, "A Wideband 2.4 GHz Delta-Sigma Fractional-N PLL With 1 Mb/s In-Loop Modulation.," *IEEE Journal of Solid State Circuits*, vol. 39, no. 1, pp. 49-62, January 2004.. [pdf]

- S. Pamarti and I. Galton., "Phase Noise Cancellation Design Tradeoffs for Delta-Sigma Fractional-N PLLs.," *IEEE Transactions on Circuits and Systems II: Analog and Digital Processing*, vol. 50, no. 11, pp. 829-838, November 2003.. [pdf]

- E. Alon, J. Kim, S. Pamarti, K. Chang, M. Horowitz., "Replica Compensated Linear Regulators for Supply-Regulated Phase Locked Loops," *IEEE Journal of Solid State Circuits*, vol. 41, no. 2, pp. 413-424, February 2006.. [pdf]

C

INDIAN INSTITUTE OF TECHNOLOGY MADRAS
Chennai 600 036, India

Shanthi Pavan
Professor of Electrical Engg

shanthi@ee.iitm.ac.in
+91 44 22574437

24th July 2016

To,
Prof.Ahmed Tewfik
Chairman, Dept. of Electrical and Computer Engg
University of Texas at Austin
Texas, USA

Reference Letter for Dr.Nan Sun

Dear Dr.Tewfik,

It is a pleasure to write this letter of reference for Dr.Nan Sun, who is an Assistant Professor in your department.

Before I begin describing Dr.Sun's excellent work, let me introduce myself. I am a full professor of Electrical Engineering at Indian Institute of Technology, Madras, where I have been working in the broad area of analog and mixed-signal integrated circuit design. I obtained my PhD from Columbia University, New York in 1999, and returned to India in 2002 to pursue a career of teaching and research after stints at Texas Instruments Inc., and Vitesse Semiconductor. I have been the Editor-in-Chief of the IEEE Transactions on Circuits and Systems:Regular Papers, and am currently a Distinguished Lecturer of the IEEE Solid State Circuits Society. More information on my work can be had from http://www.ee.iitm.ac.in/~shanthi

I first heard of Dr.Sun's work when he was a graduate student at Harvard. His PhD work, nicknamed the ``pocket NMR", made waves in the IC design community for its ingenious application of IC technology to an area finding applications in diverse fields, ranging from chemical analysis to biosensing. Dr.Sun and his colleagues' work replaced a 120kg table-top NMR system with a hand-held version. Apart from the technical aspect of the papers covering this work, what struck me was how well the papers were written. I distinctly remember, while reading Nan's papers on this subject 6 or 7 years ago, saying to myself - this author is going to go far. I am now given to understand that

this technology is being commercially exploited. The quality of his PhD work, and the resulting technology, is simply stellar.

A few years later, I became aware that Nan's work in the area of mixed signal ICs, and specifically in the area of data converters. Again, clarity of thought and elegance of exposition came through his papers, and I always looked forward to reading his papers. One such paper that specifically comes to mind is a single author paper, "High-order mismatch-shaped segmented multibit delta-sigma DACs with arbitrary unit weights," published in the IEEE Transactions on Circuits and Systems:Regular Papers. I remember this paper as I was the Associate Editor that handled this submission, and is among the top few papers I have handled as Editor. Needless to say, it was received well by the reviewers and eventually published. I believe that it was around this time that Nan started looking into the very important problem of addressing mismatch in oversampled data converters. The prior literature that existed on the subject was mostly ad hoc, and Nan's papers have made important and lasting contributions to this field, not only by proposing new techniques, but also by infusing an organic and logical development. His recent work with graduate student A.Sanyal seeks to also address the increasingly important problem of dynamic distortion in oversampled converters due to inter-symbol interference (ISI). These are difficult problems, and I am so glad to see the impressive progress made by Nan and his group in this area. I am certain that this will significantly impact the state of the art in oversampled converters. Thanks to his outstanding work in the area, Nan is well known in data-converter circles as an expert in the area. In a recent special issue on Next Generation Delta-Sigma Converters of the IEEE Journal on Emerging Techniques in Circuits and Systems (JETCAS), of which I was one of the Guest Editors, Nan was invited to contribute two papers. This issue was highly selective, with papers being contributed by invitation to experts in the field.

At this juncture, I would also like to add a few words about the research area that Nan has chosen for himself, namely data converters. This is a particularly difficult area for somebody in academia, since the competition is from large groups in industry with a long tradition, experience and know how in the area. Further, these groups consist of experienced professionals and whole groups dedicated for characterization and support. On the other hand, a fresh assistant professor has none of these advantages - there is little prior knowledge, particularly so if one's PhD is not in the data converter area. The team at one's disposal is fresh, and without the luxury of large teams to take care of the more routine stuff (like testing and characterization). Further, high resolution data converters and unforgiving of even small bugs, which can degrade performance by a few dB - making it extremely difficult to publish. It is thus no surprise that very very few professors even venture into this area, and particularly so if one is up for tenure. The risk of failure is simply too high - it is so easy to mess up a stellar idea with a small execution bug not caught by simulation. In fact, apart from Nan, I am aware of only one more assistant professor working in the area of data conversion, turning out works that pass muster in the top journals and conferences. It is much more common to find faculty working in the areas of RF, (bio)sensors etc. where the amount of effort needed for a

publication, and the risk of failure is relatively small. In this context, I find it admirable (and very brave!) that Nan has chosen to work in this area.
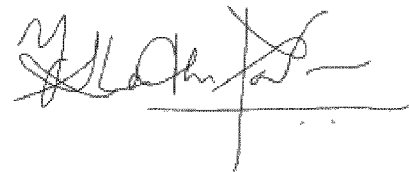
Nan has published extensively in the data converter area in the IEEE Transactions on Circuits and Systems. Many of his papers are single author works, which to me is very creditable. He has recently made much headway with SAR and VCO based analog-to-digital converters. His papers have been presented at the top conferences in the IC area, namely the Custom Integrated Circuits Conference (CICC), VLSI Circuits Symposium and the European Solid State Circuits Conference. At ESSCIRC 2016, Nan has 6 (!) papers accepted. This surely got be a record of sorts. It must be emphasized here that these conferences are highly competitive, where clever ideas MUST be demonstrated in silicon. This not only means that the designs must be executed with care, but sufficient funding must be secured to be able to fabricate these chips.

If I have to compare Nan's research output to that of others in his cohort, worldwide, I have no hesitation in saying that Nan is among the best of the best. In fact, I cannot think of any other assistant professor who has performed so well in a particularly difficult area like data-conversion. From my contacts in industry, notably from Texas Instruments, Silicon Laboratories and Analog Devices, which are leading companies in the field, I know that Nan is held in high regard by the experts in industry.

I am also sure (looking at his recent publication trajectory) that he will do exceedingly well in the future. I see him being a leader in the field, and I am personally always looking forward to reading his papers, and listening to him speak. Recognitions are coming his way - his recent appointment as Associate Editor of the IEEE Transactions on Circuits and Systems:Regular Papers is a case in point. I am sure many more brilliant students will be attracted to UT-Austin to get a chance to work with Nan.

In summary, Nan Sun is simply outstanding - I have been following his work for about 7 years now. In a less formal document, I would have said that his case for tenure is a no-brainer. Please feel free to contact me if you need any more information.

Best Regards

Shanthi Pavan

Jilda Gayle

From:	Tewfik, Ahmed H <tewfik@austin.utexas.edu>
Sent:	Sunday, July 24, 2016 8:45 AM
To:	jildagayle@gmail.com; Bearden, Carole A
Subject:	Fwd: Action needed: please let me know by 6/22 if you can provide a reference letter for Nan Sun's promotion in late July
Attachments:	NanSunLetter.pdf; ATT00001.htm

regards
Ahmed

_____

Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
1616 Guadalupe St.
UTA 7.416
Austin, TX 78701
USA

Direct: (512) 471-6179
tewfik@austin.utexas.edu

Begin forwarded message:

> **Resent-From:** <tewfik@austin.utexas.edu>
> **From:** Shanthi Pavan <shanthi@ee.iitm.ac.in>
> **Date:** July 24, 2016 at 2:17:10 PM GMT+2
> **To:** "Tewfik, Ahmed H" <tewfik@austin.utexas.edu>
> **Subject: Re: Action needed: please let me know by 6/22 if you can provide a reference letter for Nan Sun's promotion in late July**
>
> Dear Prof.Tewfik,
>
> Here is the letter of reference for Nan.
>
> Best Rgds
> Shanthi
>
> On Mon, Jun 20, 2016 at 11:22 PM, Tewfik, Ahmed H <tewfik@austin.utexas.edu> wrote:
>
>> No worries. Thanks again.
>>
>>
>>
>> Regards

1

Shanthi Pavan

Professor
Department of Electrical Engineering
Indian Institute of Technology, Madras
Chennai, 600036, India

Bio

Shanthi Pavan obtained the B.Tech degree in Electronics and Communication Engg from the Indian Institute of Technology, Madras in 1995 and the M.S and Sc.D degrees from Columbia University, New York in 1997 and 1999 respectively. From 1997 to 2000, he was with Texas Instruments in Warren, New Jersey, where he worked on high speed analog filters and data converters. From 2000 to June 2002, he worked on microwave ICs for data communication at Bigbear Networks in Sunnyvale, California. Since July 2002, he has been with the Indian Institute of Technology-Madras, where he is now a Professor of Electrical Engineering. His research interests are in the areas of high speed analog circuit design and signal processing.

Dr.Pavan is the recipient of the Shanti Swarup Bhatnagar Award in Engineering Sciences (2012), IEEE Circuits and Systems Society Darlington Best Paper Award (2009), the Swarnajayanthi Fellowship (2010, from the Government of India) , the Young Faculty Recognition Award from IIT Madras (2009, for excellence in teaching) , the Technomentor Award from the India Semiconductor Association (2010) and the Young Engineer Award from the Indian National Academy of Engineering (2006). He has been the Editor-in-Chief of the IEEE Transactions on Circuits and Systems: Part I - Regular Papers (2014-2015), and earlier served on the editorial board of the IEEE Transactions on Circuits and Systems Part II - Express Briefs (2006-2007). He is a Distinguished Lecturer of the IEEE Solid State Circuits Society and a fellow of the Indian National Academy of Engineering.

BC

Analog and Mixed-Signal Center
3128 TAMU
College Station, TX 77843-3128

Tel. (979) 845-7498
Fax. (979) 845-7161
E-mail: sanchez@ece.tamu.edu
http://www.ece.tamu.edu/~sanchez

ELECTRICAL & COMPUTER ENGINEERING
TEXAS A&M UNIVERSITY
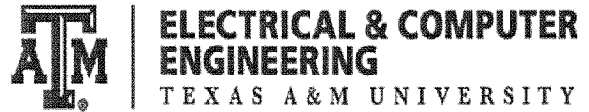
August 1, 2016

TO WHOM IT MAY CONCERN:

I am writing this letter to s support the application by **Dr. Nan Sun** for the promotion to Associate Professor at the University of Texas at Austin. Dr. Sun is a well-qualified research faculty with multidisciplinary technical background in the broad area of very low power analog/mixed signal circuits/ medical electronics. I became aware of Dr. Su's own research, and I believe he is a promising scientist. I was excited about the direction of his previous work on novel miniaturized of nuclear magnetic resonance devices in 2011 when he reported this work as a graduate student. He has several pending patents on this work and others.

He has a good record of publications before coming to UTA. After joining UT he has published 15 journal papers but 9 of them are Express Briefs or Electronic Letters. He can and should increase the number of publications in top journals. He is currently guiding 12 Ph. D students, although no one has graduated. He is often invited to give lecture and is becoming more and better recognized by his work. According to Google citations he has an h-index=12 and more than 467 citations. His most cited paper on "CMOS RF biosensor utilizing nuclear magnetic resonance" has provide a practical solution to a problem of a bulky NMR. His second most cited paper "Palm NMR and 1-chip NMR" is becoming a classical reference in this research area.

Considering his funding and 15 grants/contracts awarded as PI, his good connection with industry and the fact that has a good number of Ph. D. students with funding, plus a reasonable record of publications and citations he can become a well-established researcher if UTA continues providing a good and encouraging atmosphere for him to grow. In summary, Dr. Sun has the credentials to be promoted to Associate Professor.

If I can be of any further assistance about his promotion, please do not hesitate to contact me directly.

Sincerely,

Edgar Sánchez-Sinencio
TI J. Kilby Chair Professor and
Distinguished Professor

Edgar Sanchez-Sinencio

TI Jack Kilby Chair Professor

Distinguished Professor

Office: 318E WEB
Phone: 979.845.7498
Email: s-sanchez@tamu.edu

Personal Website
Google Scholar Profile

Research Interests

•Design and implementation of mixed-signal processing circuits and systems.

•Power Management, Medical and Environmental Applications. RF Communication Circuits.

Awards & Honors

- IEEE Fellow (92), IEEE Life Fellow (10)
- Halliburton Professorship, College of Engineering, Texas A&M University, 1993.
- IEEE Guillemin-Cauer Award, 1995.
- Honoris Causa Doctorate awarded by the National Institute for Astrophysics, Optics, and Electronics (INAOE), Mexico, November 1995.
- Texas Senate Proclamation #373 for Outstanding Accomplishments.
- IEEE Darlington Award, 1997.

- Texas Instruments Analog Engineering Chair Professor Holder , College of Engineering, Texas A&M University. March 1999- January 2002
- William & Ruth Neely/ Dow Chemical Faculty Fellow (2000-2001) Engineering Program Texas A&M University.
- IEEE Circuits and Systems Society Golden Jubilee Medal Recipient , May 2000.
- Texas Instruments/ Jack Kilby Chair Professor Holder, College of Engineering, Texas A&M University. February 2002- Present
- IEEE Circuits and Systems Society Technical Achievement Award, May 2008.
- Outstanding Professor Award 2011
- IEEE Circuits and Systems Society Distinguished Lecturer (2012-2013).
- University Distinguished Professor (2015)

Education

- Ph.D. University of Illinois, Champaign-Urbana, 1974
- M.S. Stanford University, Stanford California, 1970
- B.S. National Polytechnic Institute of Mexico, 1965

Selected Publications

J. Jin and E. Sánchez-Sinencio, "A Home Sleep Apnea Screening Device with Time-Domain Signal Processing and Autonomous Scoring Capability," IEEE Trans on Biomedical Circuits and Systems, Vol. 9 , pp. 96-104 , Issue 1, February 2015.

R. Abdullah and E. Sánchez-Sinencio, "A Biopotential Amplifier with Dynamic Capacitor Matching for Improved CMRR," Springer International Publishing, Vol. 82, Issue1, pp. 47-55, 2014.

C. Erbay, S. Carreon Bautista, E. Sánchez-Sinencio, and A. Han, "High Performance Monolithic Power Management System with Dynamic Maximum Power Point Tracking for Microbial Fuel Cells," ACS Publications, Environmental Science & Technology, pp. 1-25, November 3, 2014.

S. Carreon-Bautista, S.; Eladawy, A.; Nadar Mohieldin, A.; Sanchez-Sinencio, E., "Boost Converter with Dynamic Input Impedance Matching for Energy Harvesting with Multi-Array Thermoelectric Generators," IEEE Transactions on Industrial Electronics, Vol. 61, No. 10, pp. 5345-5353, October 2014.

OSU
Oregon State
UNIVERSITY

Gabor C. Temes, Professor
School of Electrical Engineering and Computer Science
Oregon State University, 4103 Kelley Engineering Center, Corvallis, OR 97331-5501
Phone: 541-737-2979 | Fax: 541-737-1300 | Email: temes@eecs.oregonstate.edu

C

July 5, 2016

Re: Prof. Nan Sun

Dear Prof. Tewfik,

In reply to your letter of June 21, 2016, I am pleased to provide my assessment of Dr. Nan Sun's research contributions. In answer to your questions,

1. I have known Dr. Sun for some years. I have read several of his publications during the past 5–6 years. Also, I visited UT Austin last August to give a seminar, and Prof. Sun was my host. In turn, this April he delivered a widely attended and very successful seminar at my school.

2. Prof. Sun's past research extended over a wide area. I am most familiar with his work on mismatch shaping of multibit DACS and other digital correction methods used in analog integrated circuits. His papers on these topics describe mathematically sophisticated and also practically useful algorithms and circuits. I am sure that they had a wide influence in the field – they certainly impressed and influenced our group here.

3. I found Dr. Sun's productivity highly impressive. The number of his publications in highly-regarded and selective journals and conferences is very high. The additional book chapters and patent applications listed make the record even more striking.

4. Extrapolating from the 5-year record of Prof. Sun, I predict an exceptionally successful future career for him.

I hope that this information was helpful. I shall be glad to answer additional questions if needed.

Sincerely,

Gabor C. Temes
Professor, Oregon State University
3091 Kelley Engineering Center
Corvallis, OR 97331-5501

Jilda Gayle

From:	Tewfik, Ahmed H <tewfik@austin.utexas.edu>
Sent:	Tuesday, July 5, 2016 5:04 PM
To:	Bearden, Carole A; Jilda Bolton
Subject:	FW: Dr. Nan Sun
Attachments:	20160705144617095.pdf
Signed By:	tewfik@austin.utexas.edu

FYI

Regards
Ahmed

-----Original Message-----
From: Temes, Gabor [mailto:Gabor.Temes@oregonstate.edu]
Sent: Tuesday, July 5, 2016 4:54 PM
To: Tewfik, Ahmed H <tewfik@austin.utexas.edu>
Cc: "temes' (temes@eecs.oregonstate.edu)' <temes@eecs.oregonstate.edu>
Subject: Dr. Nan Sun

Dear Ahmed,

Please find attached my reference on Nan Sun.

Best regards,

Gabor

1

Electrical Engineering and Computer Science

Gabor C. Temes
Distinguished Emeritus Professor
Primary Area: Physical and Wave Electronics

Research Areas
Data converters; switched-capacitor circuits; analog and digital signal processing

Research Description
Communications, instrumentation, consumer electronics, etc. are all increasingly relying on digital signal processing (DSP) to carry out complex and time-consuming tasks. However, unavoidably, the input and output signals to all such systems had to remain analog, since signals encountered in nature are analog. Hence, interfaces are needed between the DSP core and the input/output terminals of all such systems, to process analog signals and to convert analog and digital signals into each other. With DSP technology exponentially improving in terms of speed, complexity and accuracy, the state of interface electronics has been left behind.

Temes was elected to the National Academy of Engineering in 2015.

A Life Fellow of IEEE, Temes served as associate editor of the Journal of the Franklin Institute, editor of the IEEE Transactions on Circuit Theory, and vice president of the IEEE Circuits and Systems Society (CAS). In 1968 and 1981 he was co-winner of the CAS Darlington Award, and in 1984 winner of the Centennial Medal of the IEEE. He received the Andrew Chi Prize Award of the IEEE Circuits and Systems Society of 1987, the Technical Achievement Award in 1998, the Millennium Medal and IEEE CAS Golden Jubilee Medal in 2000. Temes was also the recipient of the IEEE Gustave Kirchhoff Award in 2006, the IEEE CAS Mac Van Valkenburg Award in May 2009, and OSU College of Engineering Research Award in 2010.